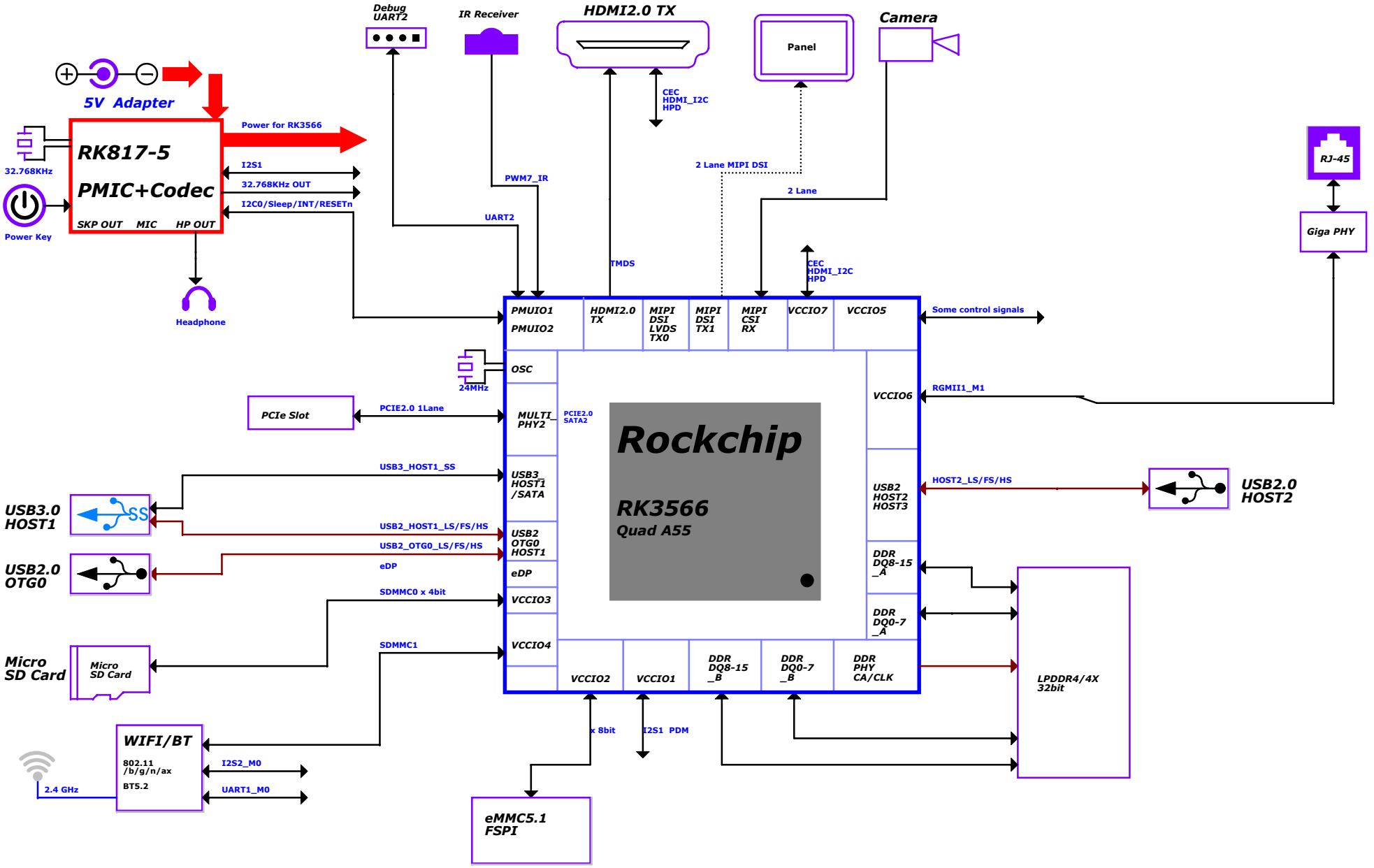
Revision History

Version	Date	By	Change Dsecription	Approved
1.0	2024/04/28		Released for production	

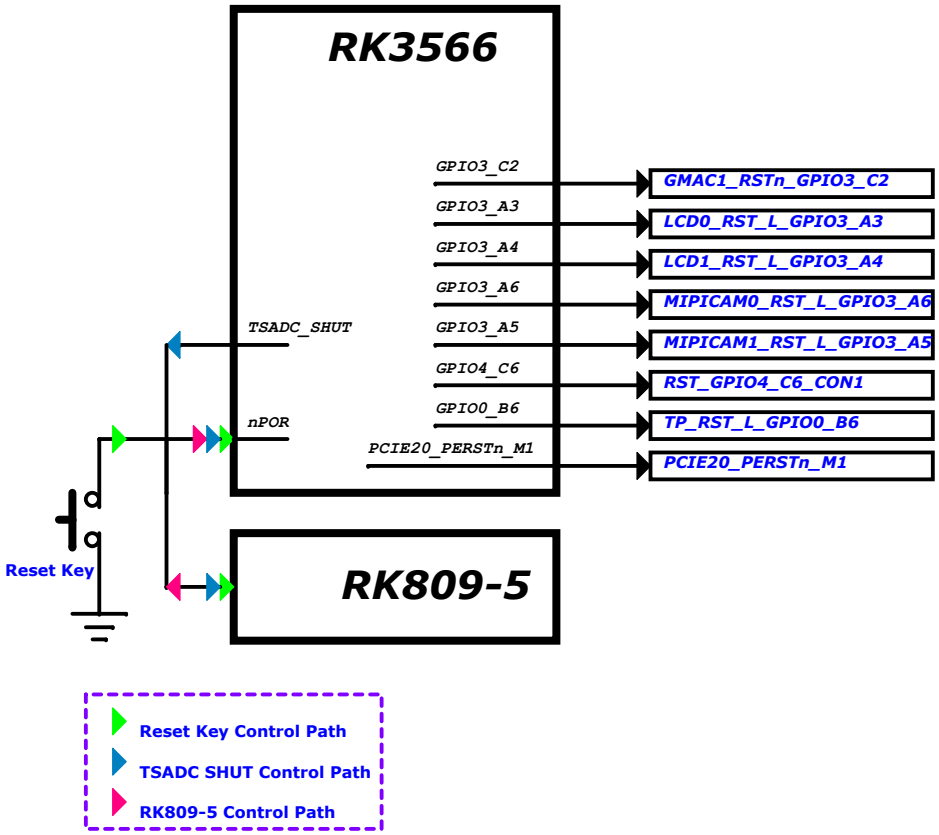
PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	01.Revision History				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	1 of 30

RK3566 Ref Block Diagram

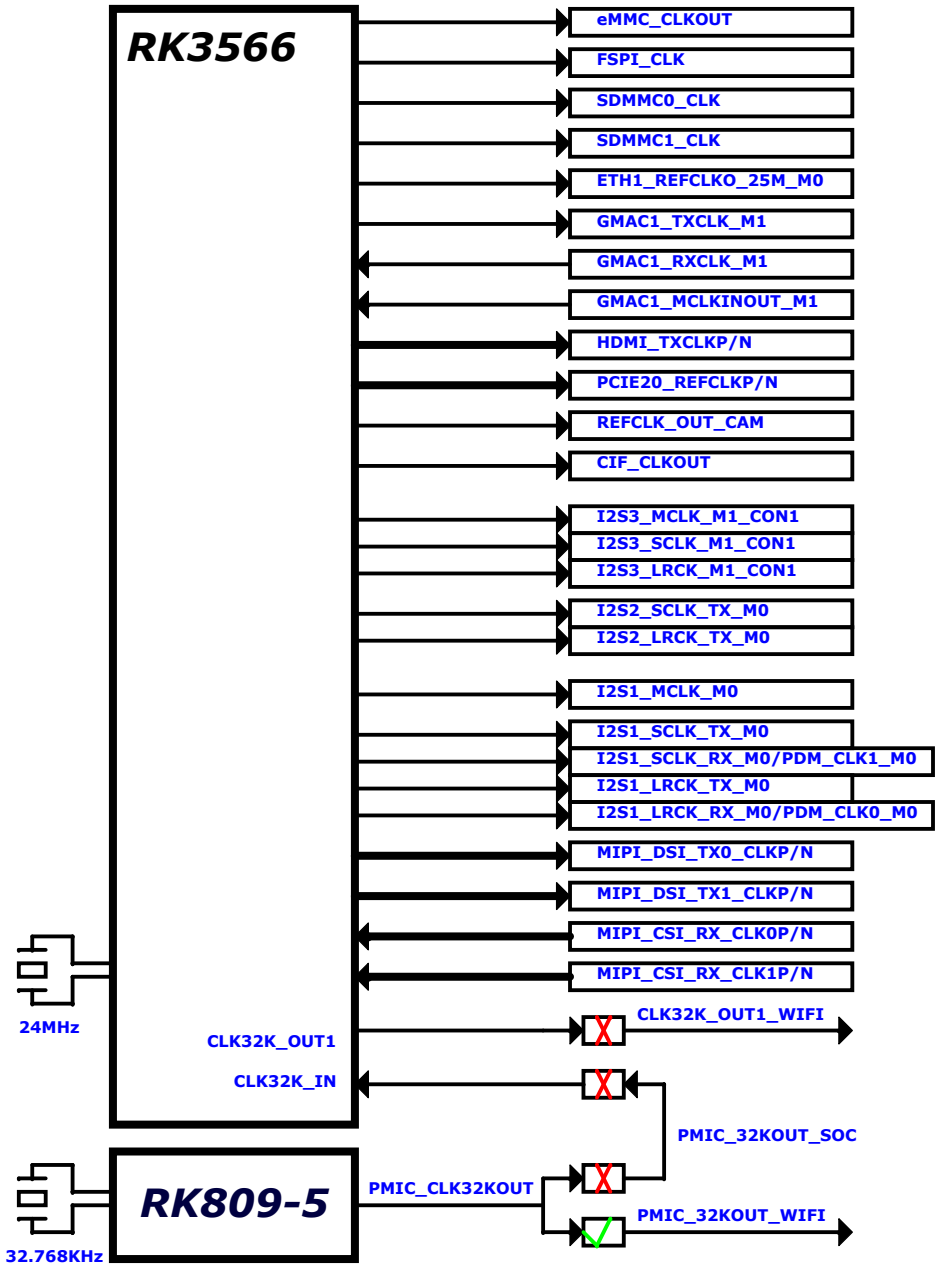


PINE64	PINE64
Project:	Quartz64 Zero Schematic-20240428
File:	02.Block Diagram
Date:	Tuesday, March 26, 2024
Rev:	V1.6
Designed by:	Daniel_J
Reviewed by:	Default
Sheet:	2 of 30

RESET Signal MAP

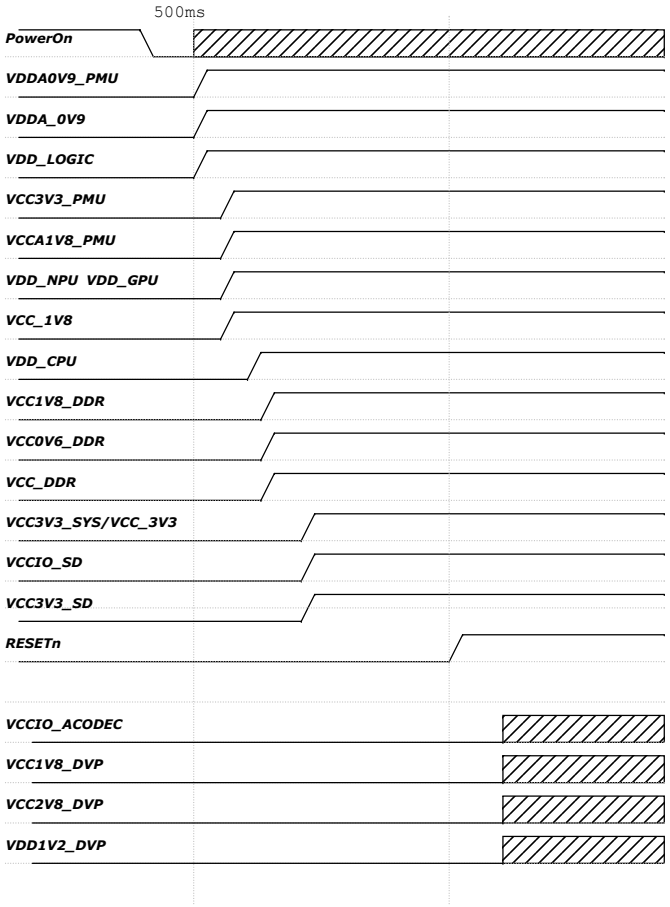


Clock Map



PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	04.Reset Map/Clock Map				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	3 of 30

Power Sequence &Power Path assignment



Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC_SYS	RK817-5_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF
VCC_SYS	RK817-5_BUCK2	2.5A	VDD_NPU,VDD_GPU	Slot:2	0.9V	ON	OFF
VCC_SYS	RK817-5_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC_SYS	RK817-5_BUCK4	1.5A	VCC3V3_SYS	Slot:4	3.3V	ON	OFF
VCC_SYS	RK817-5_LDO1	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK817-5_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK817-5_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_LDO4	0.4A	VCCIO_ACODEC	N/A	--/3.3V	ON	OFF
	RK817-5_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK817-5_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC_SYS	RK817-5_LDO7	0.4A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK817-5_LDO8	0.4A	VCC1V8_DVP	N/A	--/1.8V	ON	OFF
	RK817-5_LDO9	0.4A	VCC2V8_DVP	N/A	--/2.8V	ON	OFF
VCC_BAT	RK817-5_RESETn			Slot:4+5			
VCC_BAT	RK817-5_BOOST RK817-5_OTG	1.5A	VCC5V_MIDU VBUS	N/A	--/5.0V	ON	OFF
VCC3V3_SYS	Switch		VCC_3V3	Slot:4	3.3V	ON	OFF
VCC3V3_SYS	Switch		VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF
VCC_SYS	EXT BUCK	2A	VDD1V2_DVP	N/A	--/1.2V	ON	OFF

IO Power Domain Map

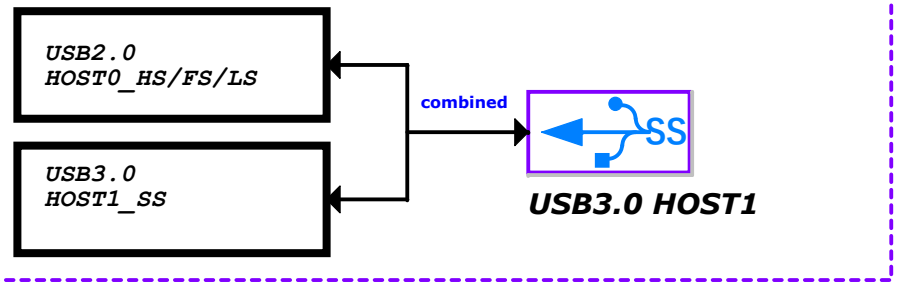
Refer to the actual design!

IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCCA1V8_PMU	VCCA1V8_PMU	1.8V/*3.3V	1.8V as default, dts config should follow the HW design
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO_WL	VCC_1V8	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_1V8	1.8V	
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC1V8_DVP	1.8V	
VCCIO7	1N8	YES	YES	VCCIO7	VCC_3V3	3.3V	

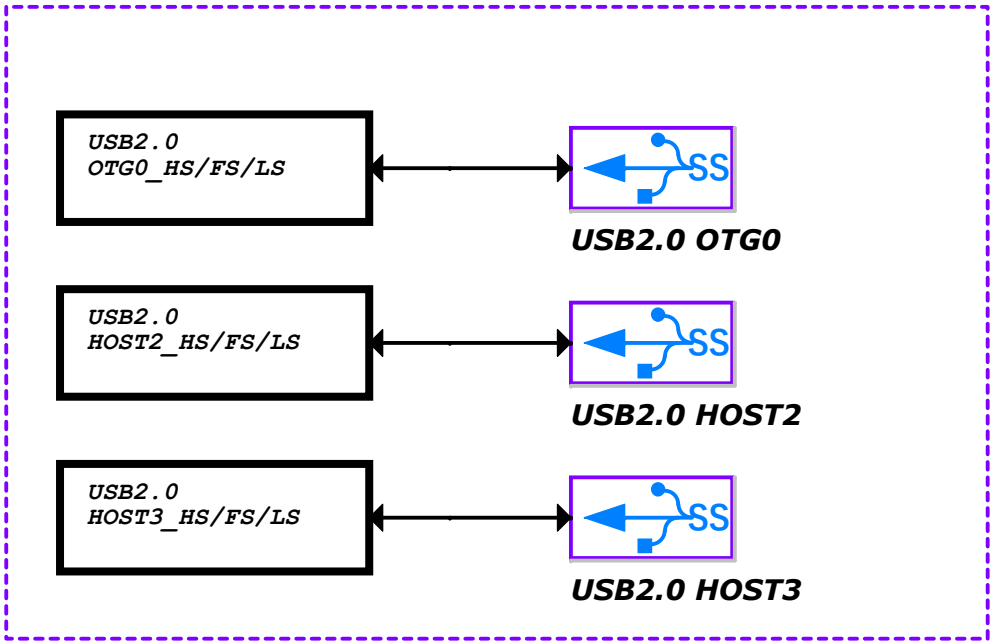
PINE64 PINE64

Project:	Quartz64 Zero Schematic-20240428				
File:	03.Power Sequence/IO Domain Map				
Date:	Tuesday, March 26, 2024			Rev:	V1.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	4 of 30

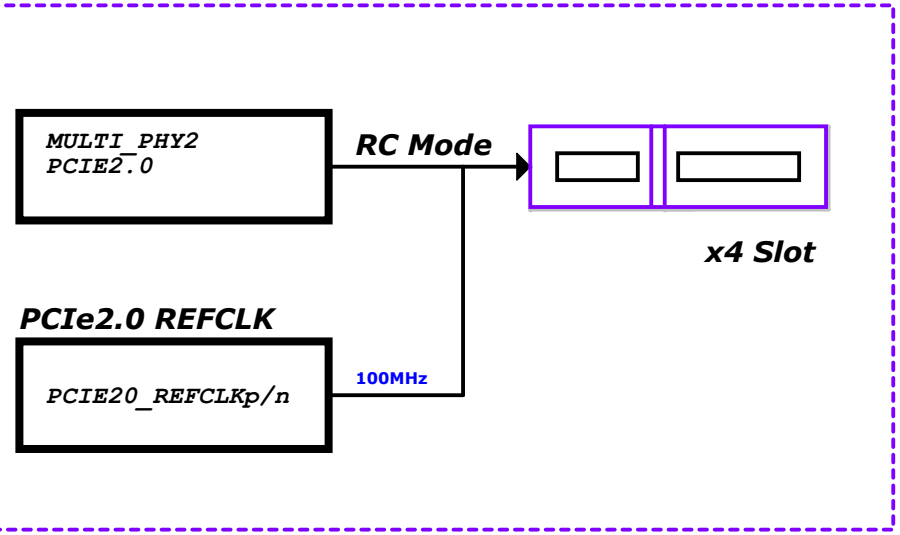
USB3.0 HOST1



USB2.0 OTG0/HOST2/HOST3



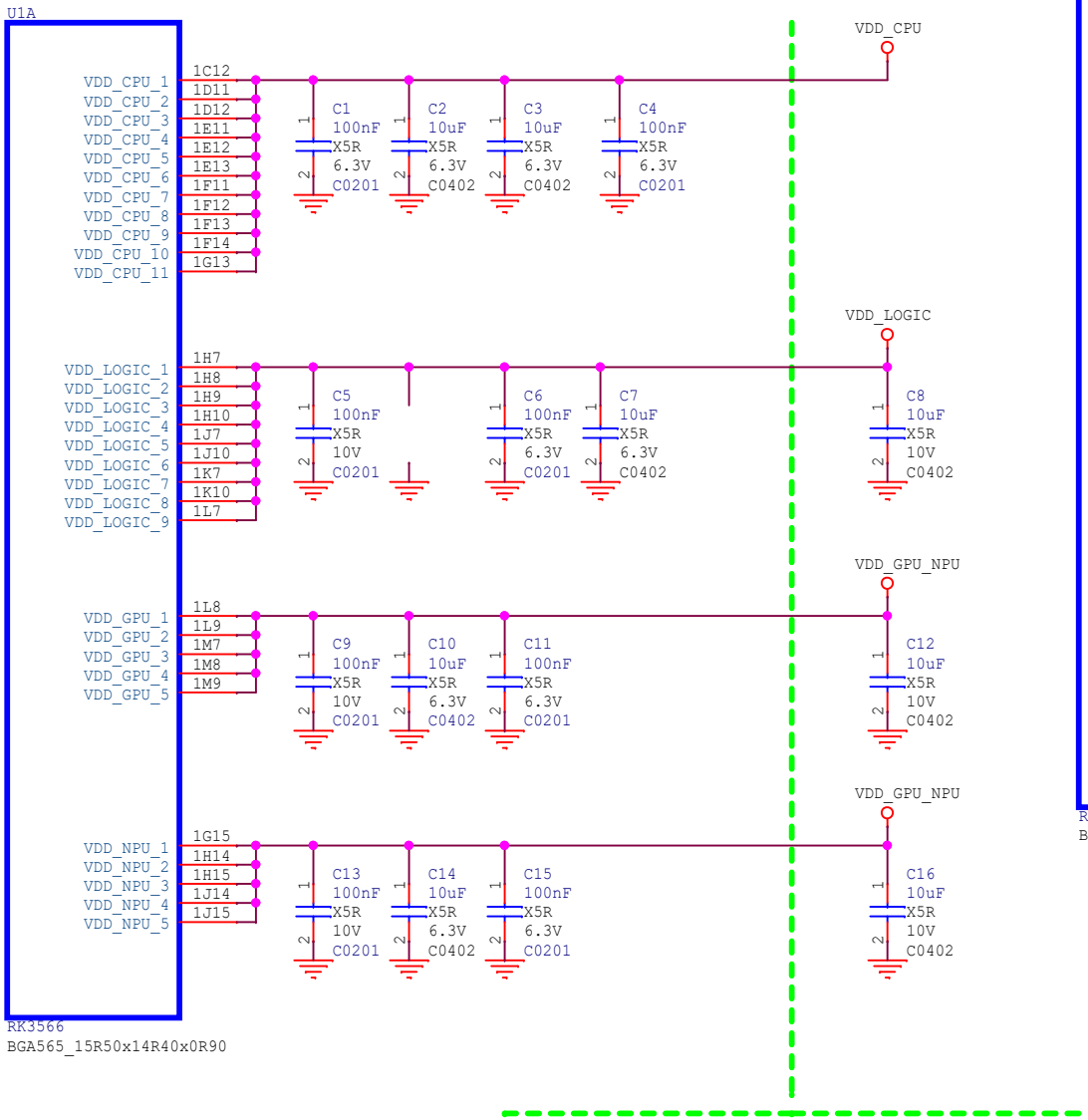
PCIE2.0 x1 Lane

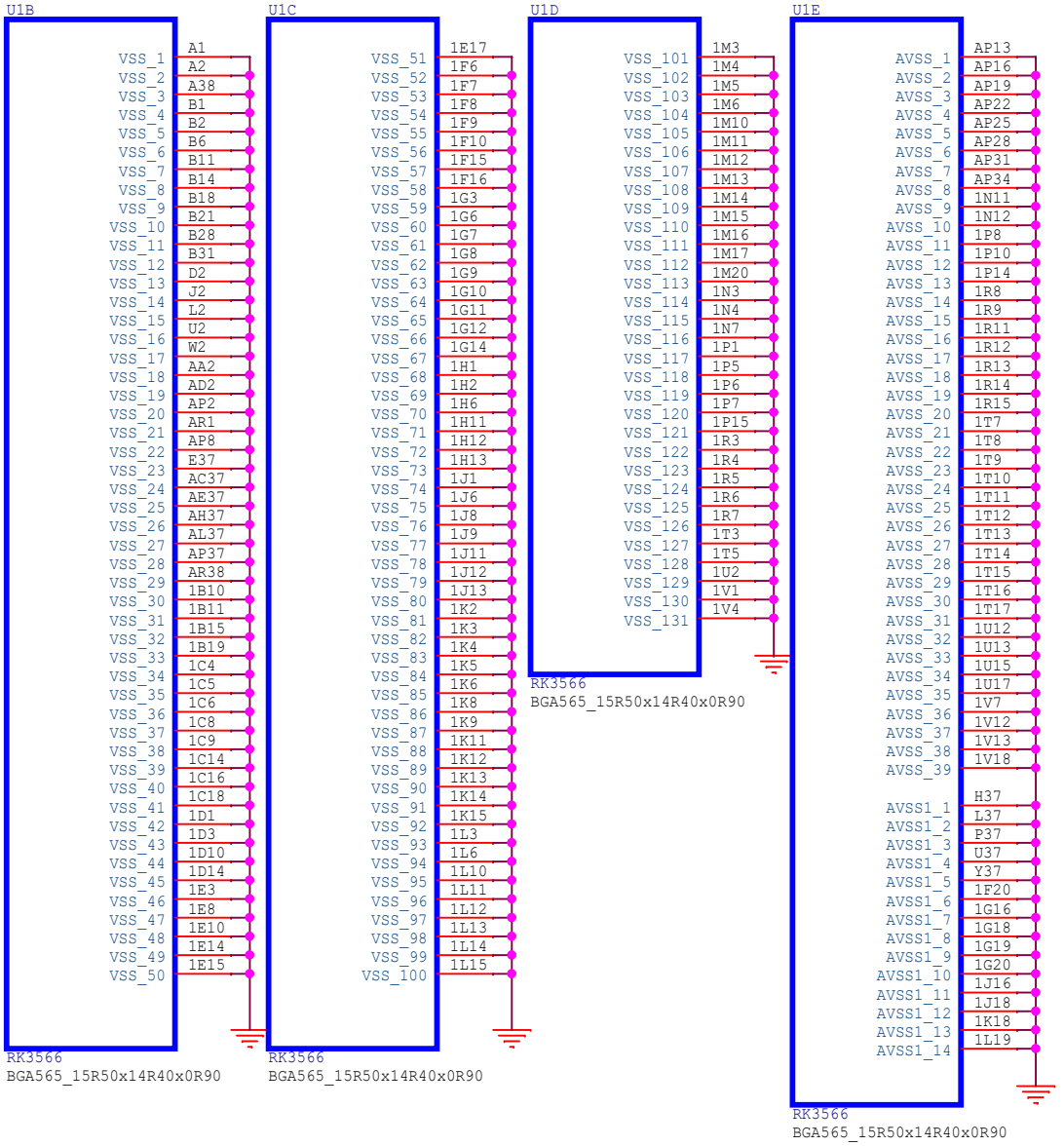


PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	07.USB/PCIE Function Map				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	DanielJ	Reviewed by:	Default	Sheet:	5 of 30

RK3566_ABCDE

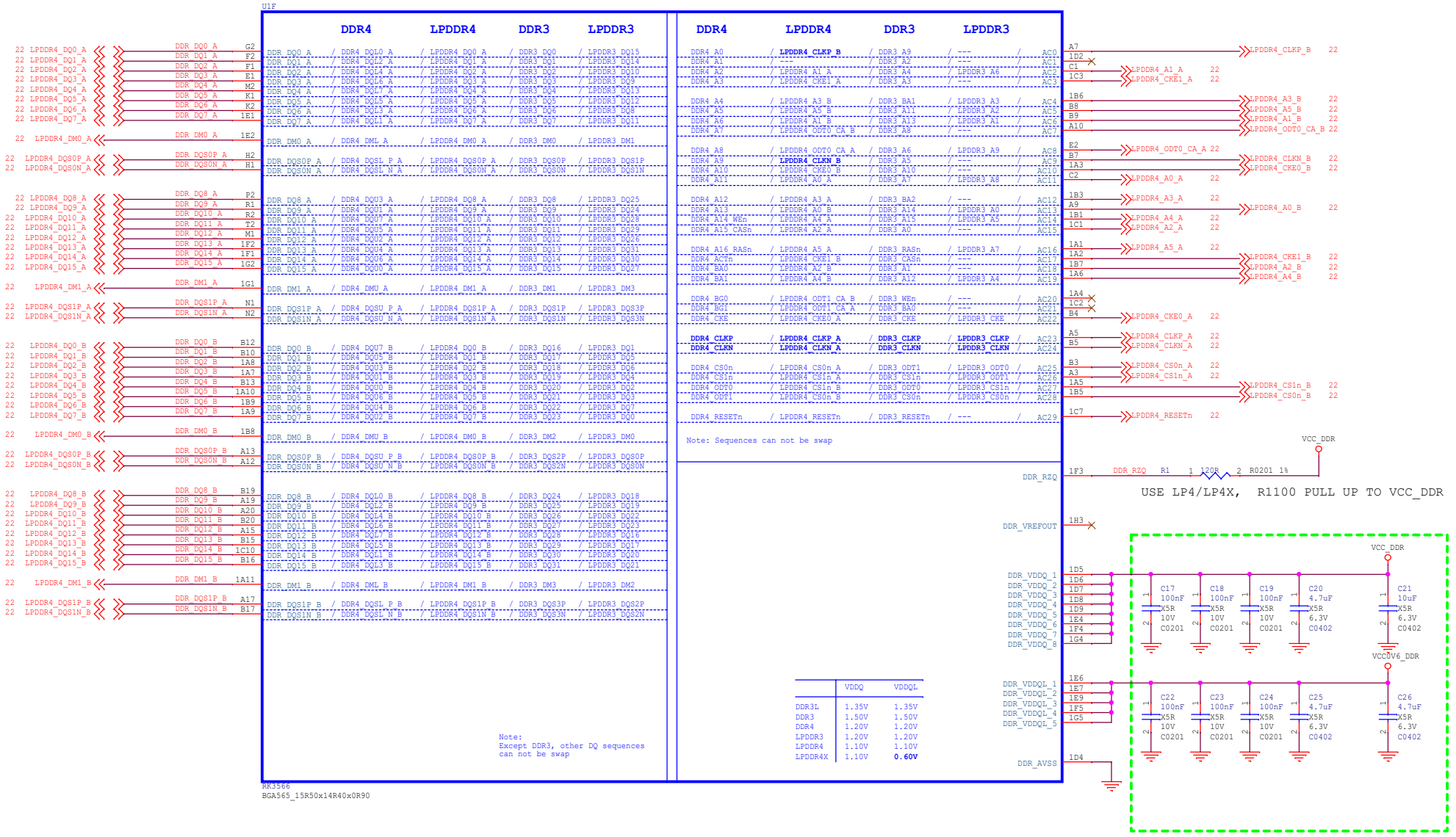
(Power&GND)





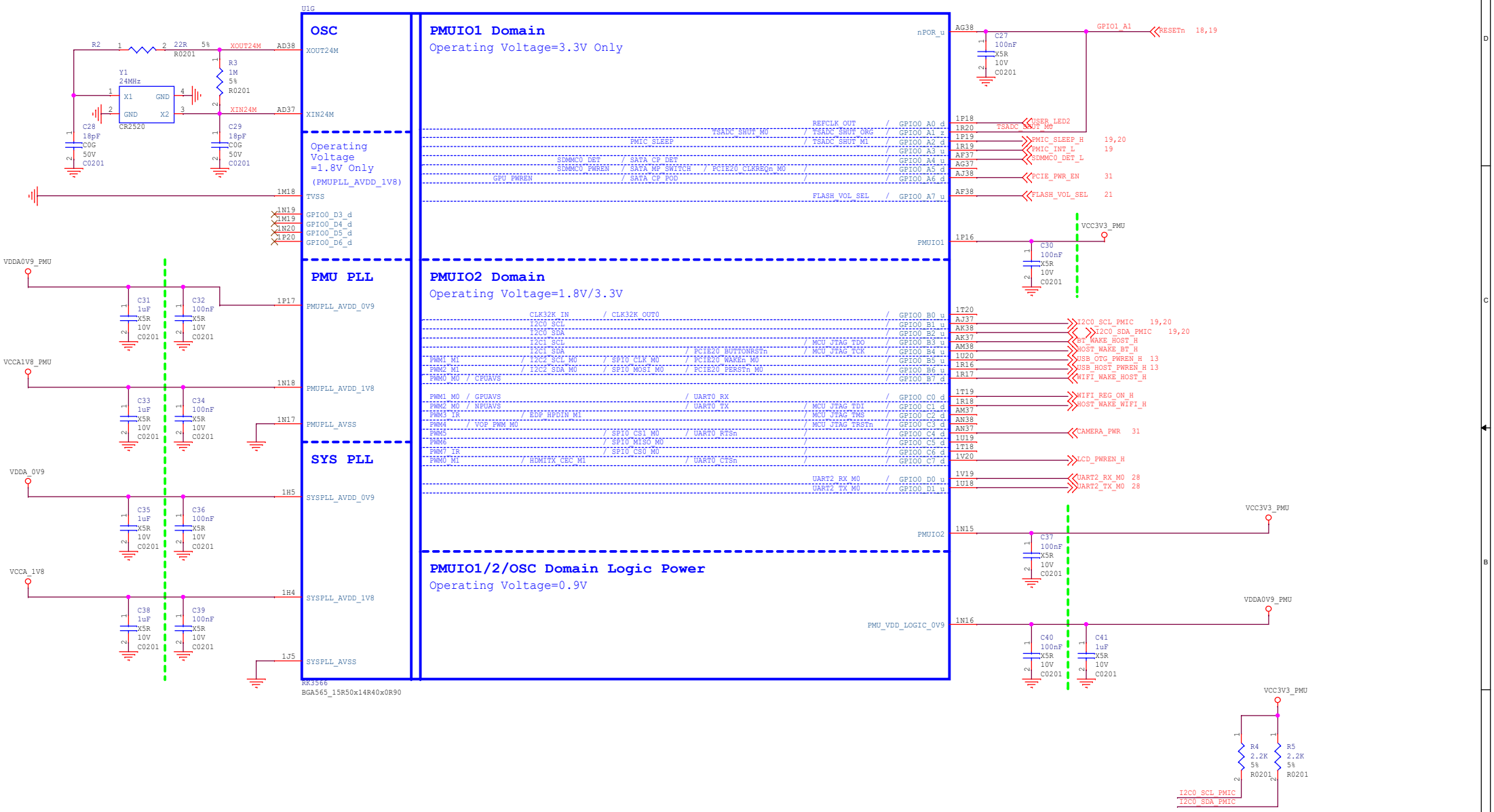
PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	08.RK3566_Power/GND				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	6 of 30

RK3566_F(DDR PHY)



PINE64	PINE64
Project:	Quartz64 Zero Schematic-20240428
File:	09.RK3566_DDR PHY
Date:	Tuesday, March 26, 2024
Rev:	V1.0
Designed by:	Daniel.J
Reviewed by:	Default
Sheet:	7 of 30

RK3566_G(OSC/PLL/PMUIO1/2)



PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	10.RK3566_OSC/PLL/PMUIO				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	8 of 30

RK3566_I(VCCIO2 Domain)

U1I

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

EMMC_D0	/ FLASH_D0	/ GPIO1_B4_u	A32	eMMC_D0	23
EMMC_D1	/ FLASH_D1	/ GPIO1_B5_u	B27	eMMC_D1	23
EMMC_D2	/ FLASH_D2	/ GPIO1_B6_u	B32	eMMC_D2	23
EMMC_D3	/ FLASH_D3	/ GPIO1_B7_u	B29	eMMC_D3	23
EMMC_D4	/ FLASH_D4	/ GPIO1_C0_u	B33	eMMC_D4	23
EMMC_D5	/ FLASH_D5	/ GPIO1_C1_u	A30	eMMC_D5	23
EMMC_D6	/ FLASH_D6	/ GPIO1_C2_u	B30	eMMC_D6	23
EMMC_D7	/ FLASH_D7	/ GPIO1_C3_u	A33	eMMC_D7	23
EMMC_CMD	/ FLASH_WRn	/ GPIO1_C4_u	A27	eMMC_CMD	23
EMMC_CLKOUT	/ FLASH_DQS	/ GPIO1_C5_d	A29	eMMC_CLKOUT	23
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/ GPIO1_C6_d	1A16	eMMC_DATA_STROBE	23
EMMC_RSTn	/ FSPI_D2 / FLASH_WPn	/ GPIO1_C7_d	1B16	eMMC_RSTn/FSPI_D2	18
	FSPI_CLK / FLASH_ALE	GPIO1_D0_d	1A15	FSPI_CLK	
	FSPI_D0 / FLASH_RDY	GPIO1_D1_u	1A17	FSPI_D0	
	FSPI_D1 / FLASH_RDn	GPIO1_D2_u	1A18	FSPI_D1	
	FSPI_CS0n / FLASH_CS0n	GPIO1_D3_u	1B17	FSPI_CS0n	
	FSPI_D3 / FLASH_CS1n	GPIO1_D4_u	1C15	FSPI_D3	

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

RK3566
BGA565_15R50x14R40x0R90

VCCIO2 1C13 — C42 100nF X5R 10V C0201 — VCCIO_FLASH

R8 1 2 22R 5% R0201

VCC_SPIFLASH — R4300 10K 5% R0201 — eMMC_RSTn/FSPI_D2

VCC_SPIFLASH — R4301 10K 5% R0201 — FSPI_D3

default VCC = 1.8V

U4300
GD25LQ255EWIG
wson8_6x5

FSPI_CS0n	1	CS	VCC 8
FSPI_D1	2	DO(D1)	HOLD(D3) 7 FSPI_D3
eMMC_RSTn/FSPI_D2	3	WP(D2)	CLK 6 FSPI_CLK
	4	VSS	DI(D0) 5 FSPI_D0
		GND 9	

VCC_SPIFLASH — C4300 100nF X5R 10V C0201 — C4301 1uF X5R 6.3V C0201 — R4302 1 2 0R 1% R0402 — VCCIO_FLASH

RK3566_J(VCCIO3 Domain)

U1J

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

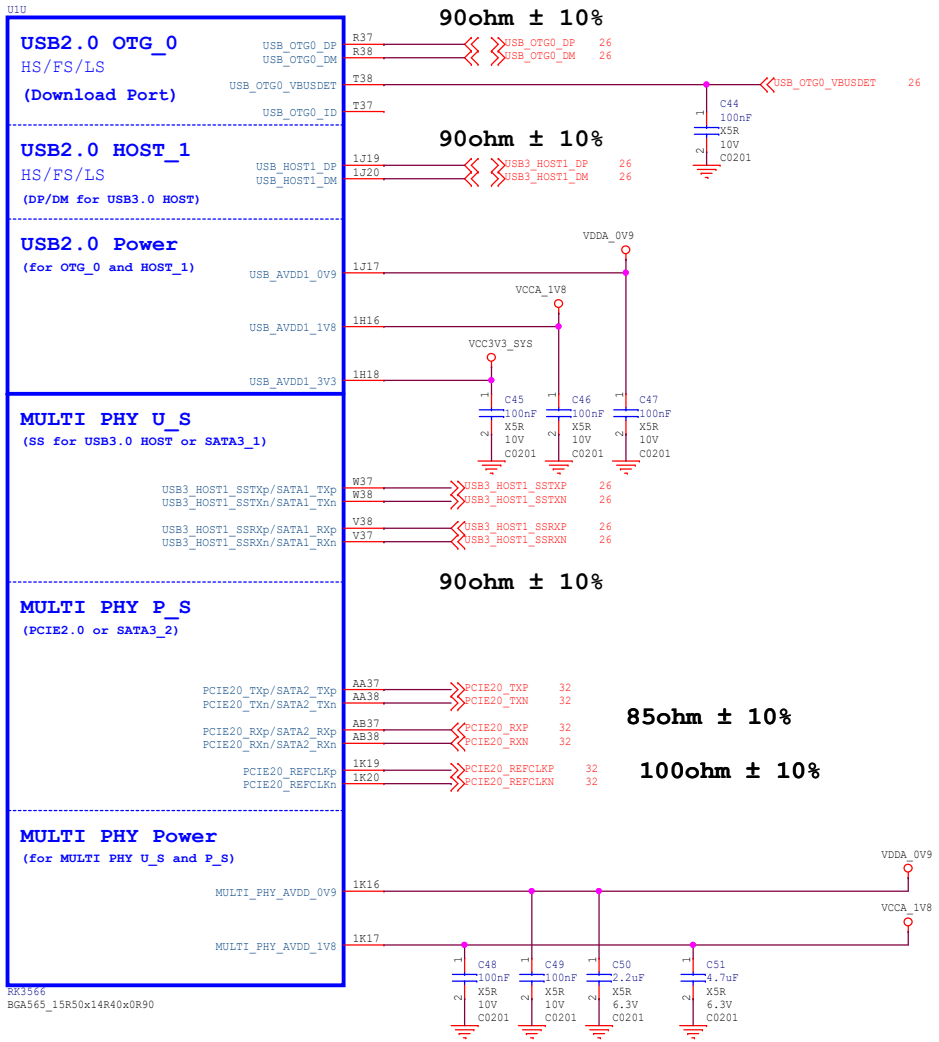
PWM8_M1	/ SDMMC0_D0 / UART2_TX_M1 / UART6_TX_M1	/ GPIO1_D5_u	1E20	SDMMC0_D0	SDMMC0_D0 18
PWM9_M1	/ SDMMC0_D1 / UART2_RX_M1 / UART6_RX_M1	/ GPIO1_D6_u	1F19	SDMMC0_D1	SDMMC0_D1 18
	SDMMC0_D2 / ARM_JTAG_TCK / UART5_CTSn_M0	/ GPIO1_D7_u	1D20	SDMMC0_D2	SDMMC0_D2 18
	SDMMC0_D3 / ARM_JTAG_TMS / UART5_RTSn_M0	/ GPIO2_A0_u	1F18	SDMMC0_D3	SDMMC0_D3 18
PWM10_M1	/ SDMMC0_CMD / UART5_RX_M0	/ GPIO2_A1_u	1E19	SDMMC0_CMD	SDMMC0_CMD 18
	SDMMC0_CLK / TEST_CLKOUT / UART5_TX_M0	/ GPIO2_A2_d	G38	SDMMC0_CLK	SDMMC0_CLK 18

RK3566
BGA565_15R50x14R40x0R90

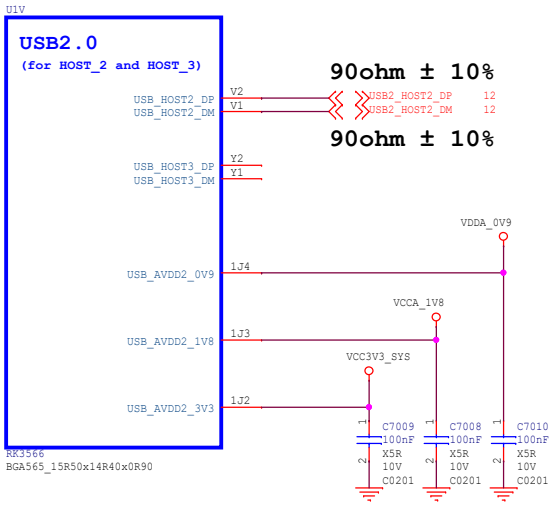
VCCIO3 1F17 — C43 100nF X5R 10V C0201 — VCCIO_SD

PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	11.RK3566_Flash/SD Controller				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	9 of 30

RK3566_U(USB3.0/PCIe2.0 x1)

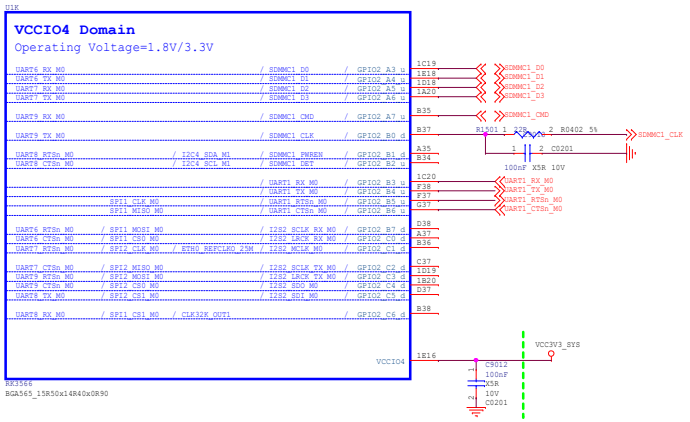


RK3566_V(USB2.0 HOST)

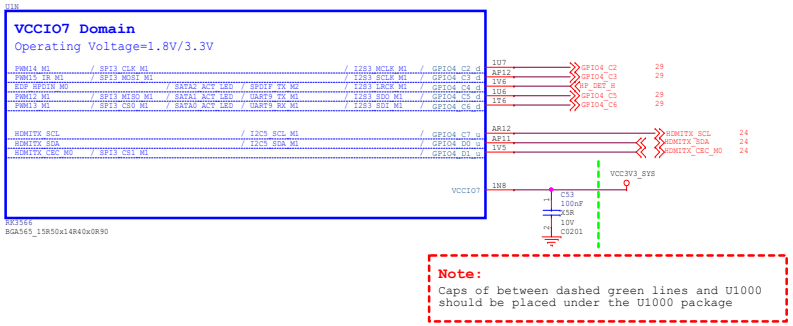


PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	12.RK3566_USB/PCIe PHY				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	10 of 30

RK3566_K(VCCIO4 Domain)

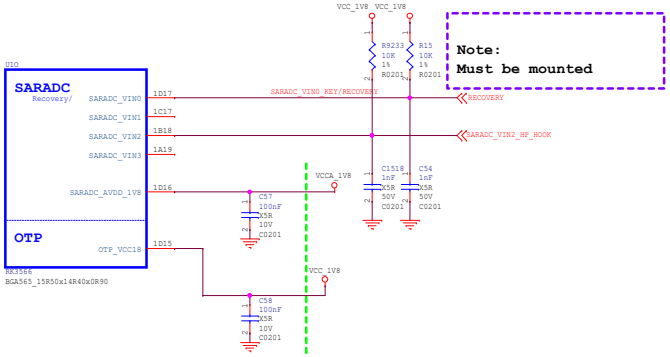


RK3566_N(VCCIO7 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

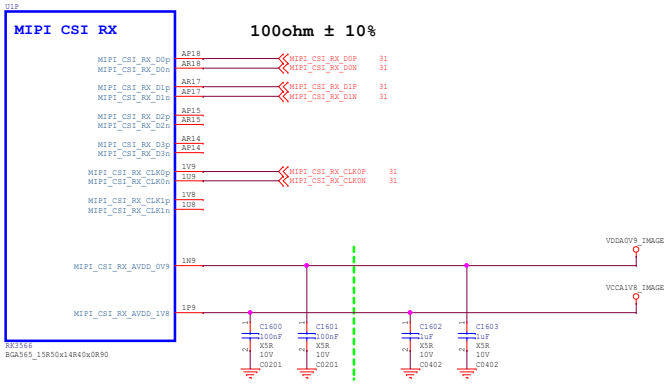
RK3566_O(SARADC/OTP)



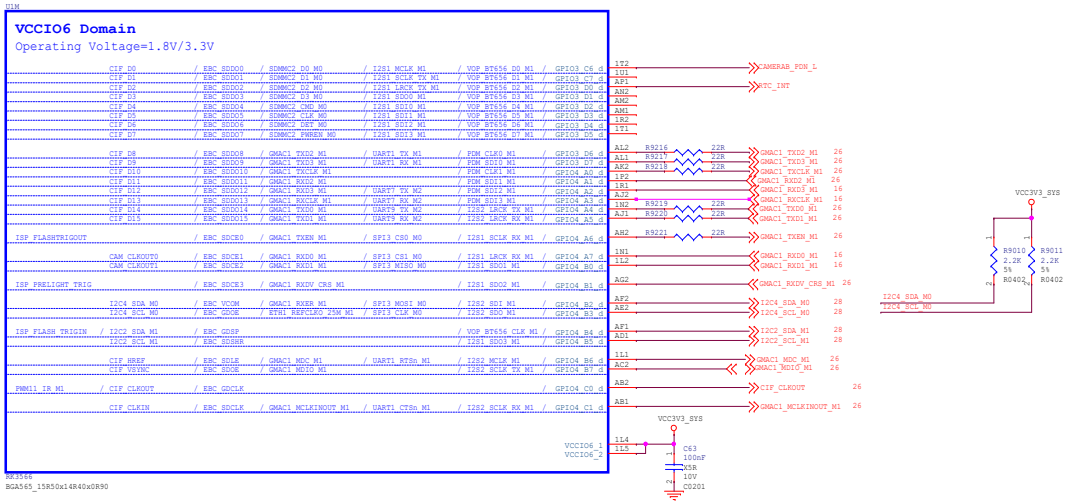
Note:
Must be mounted

PINE64	PINE64			
Project:	Quartz64 Zero Schematic-20240428			
File:	13.RK3566_SARADC/GPIO			
Date:	Monday, April 22, 2024		Rev:	V1.0
Designed by:	Daniel_J	Reviewed by:	Default	Sheet: 11 of 30

RK3566_P(MIPI_CSI_RX)

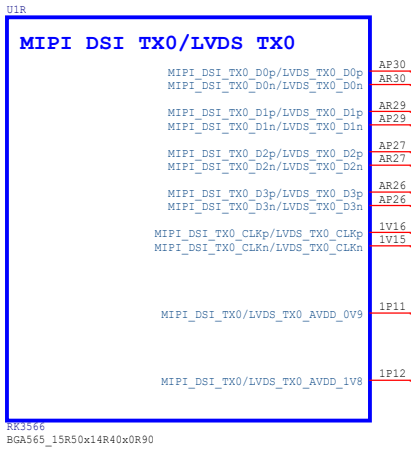


RK3566_M(VCCIO6 Domain)

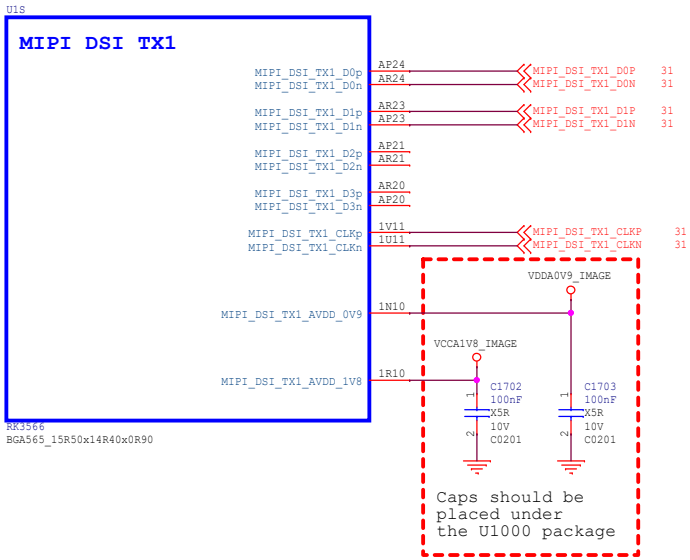


PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	14.RK3566_VI Interface				
Date:	Friday, April 26, 2024			Rev:	V1.0
Designed by:	Daniel_J	Reviewed by:	Default	Sheet:	12 of 30

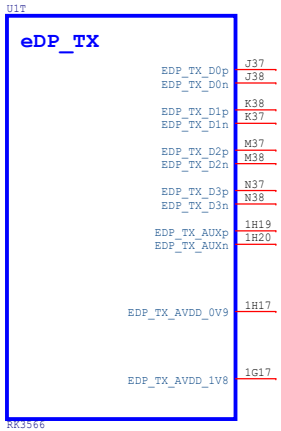
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



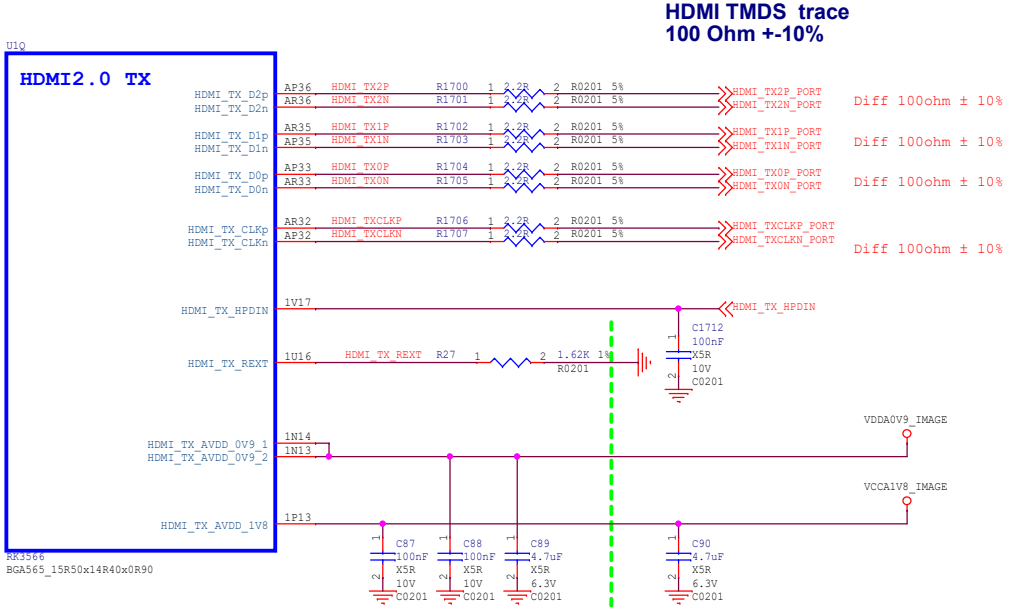
RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP TX)



RK3566_Q(HDMI2.0 TX)



PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	15.RK3566_VO Interface_1				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	13 of 30

U1L

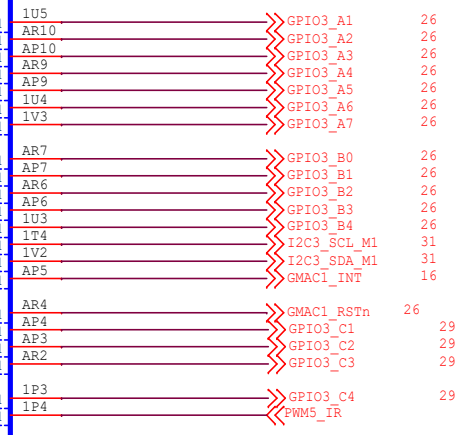
VCCIO5 Domain

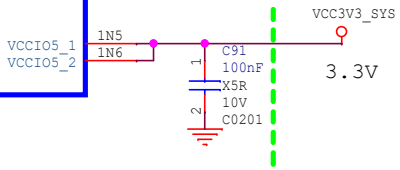
Operating Voltage=1.8V/3.3V

	VOP_BT1120_D0	/ SPI1_CS0_M1			/ SDMMC2_D0_M1	/ GPIO3_A1_d
	VOP_BT1120_D1		/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
	VOP_BT1120_D2		/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
	VOP_BT1120_D3		/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
	VOP_BT1120_D4		/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
	VOP_BT1120_CLK		/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
	VOP_BT1120_D5		/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
	VOP_BT1120_D6		/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
PWM8_M0	/ VOP_BT1120_D7		/ GMAC1_RXD0_M0	/ UART4_RX_M1		/ GPIO3_B1_d
PWM9_M0	/ VOP_BT1120_D8		/ GMAC1_RXD1_M0	/ UART4_TX_M1		/ GPIO3_B2_d
	VOP_BT1120_D9	/ I2C5_SCL_M0	/ GMAC1_RXDV_CRS_M0		/ PDM_SDI0_M2	/ GPIO3_B3_d
	VOP_BT1120_D10	/ I2C5_SDA_M0	/ GMAC1_RXER_M0		/ PDM_SDI1_M2	/ GPIO3_B4_d
PWM10_M0	/ VOP_BT1120_D11	/ I2C3_SCL_M1	/ GMAC1_TXD0_M0			/ GPIO3_B5_d
PWM11_IR_M0	/ VOP_BT1120_D12	/ I2C3_SDA_M1	/ GMAC1_TXD1_M0			/ GPIO3_B6_d
PWM12_M0			/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
PWM13_M0			/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
	VOP_BT1120_D13	/ SPI1_MOSI_M1		/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
	VOP_BT1120_D14	/ SPI1_MISO_M1		/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
	VOP_BT1120_D15	/ SPI1_CLK_M1		/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0		/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0		/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

RK3566

BGA565_15R50x14R40x0R90





PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	16.RK3566_VO Interface_2				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	14 of 30

RK3566_H(VCCIO1 Domain)

U1H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

	/ I2C3_SDA_M0	/ UART3_RX_M0	/ AUDIOPWM_LOUT_p	/ GPIO1_A0_u	A22 → GPIO1_A0
	/ I2C3_SCL_M0	/ UART3_TX_M0	/ AUDIOPWM_LOUT_n	/ GPIO1_A1_u	B22 → GPIO1_A1
SCR_CLK	/ I2S1_MCLK_M0	/ UART3_RTSn_M0		/ GPIO1_A2_d	A23 → I2S1_MCLK_M0_RK817
SCR_IO	/ I2S1_SCLK_TX_M0	/ UART3_CTSn_M0		/ GPIO1_A3_d	B23 → I2S1_SCLK_TX_M0_RK817
	I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0 / SPDIF_TX_M0	/ GPIO1_A4_d	1A13 → GPIO1_A4
SCR_RST	/ I2S1_LRCK_TX_M0	/ UART4_RTSn_M0		/ GPIO1_A5_d	B24 → I2S1_LRCK_TX_M0_RK817
	I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0 / AUDIOPWM_ROUT_p	/ GPIO1_A6_d	1A14
SCR_DET	/ I2S1_SDO0_M0	/ UART4_CTSn_M0	/ AUDIOPWM_ROUT_n	/ GPIO1_A7_d	B25 → I2S1_SDO0_M0_RK817
	I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0 / PCIE20_CLKREQn_M2	/ GPIO1_B0_d	1B13 → PCIE_CLKREQ_N 32
	I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0 / PCIE20_WAKEn_M2	/ GPIO1_B1_d	A26 → PCIE_DET_WAKE 32
	I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0 / PCIE20_PERSTn_M2	/ GPIO1_B2_d	B26 → PCIE_RST_B 32
		I2S1_SDI0_M0	/ PDM_SDI0_M0	/ GPIO1_B3_d	1B14 → I2S1_SDI0_M0/PDM_SDI0_M0_RK817

VCCIO1 — 1D13

VCCIO_ACODEC

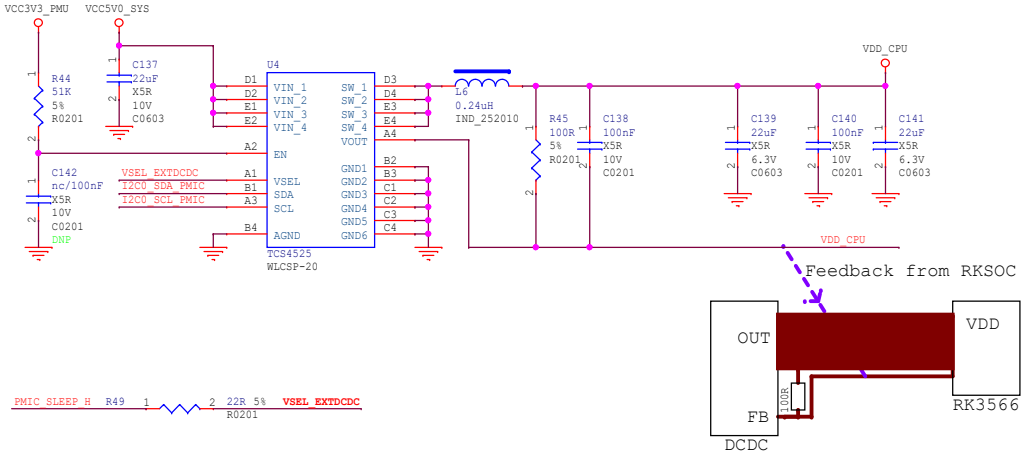
C92
100nF
X5R
10V
C0201

RK3566
BGA565_15R50x14R40x0R90

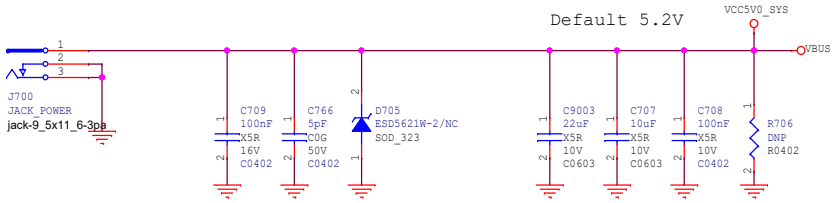
PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	17.RK3566_Audio Interface				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	15 of 30

I2C0_SCL_PMIC 10,19
I2C0_SDA_PMIC 10,19
PMIC_SLEEP_H 10,19

VDD_CPU_EXT



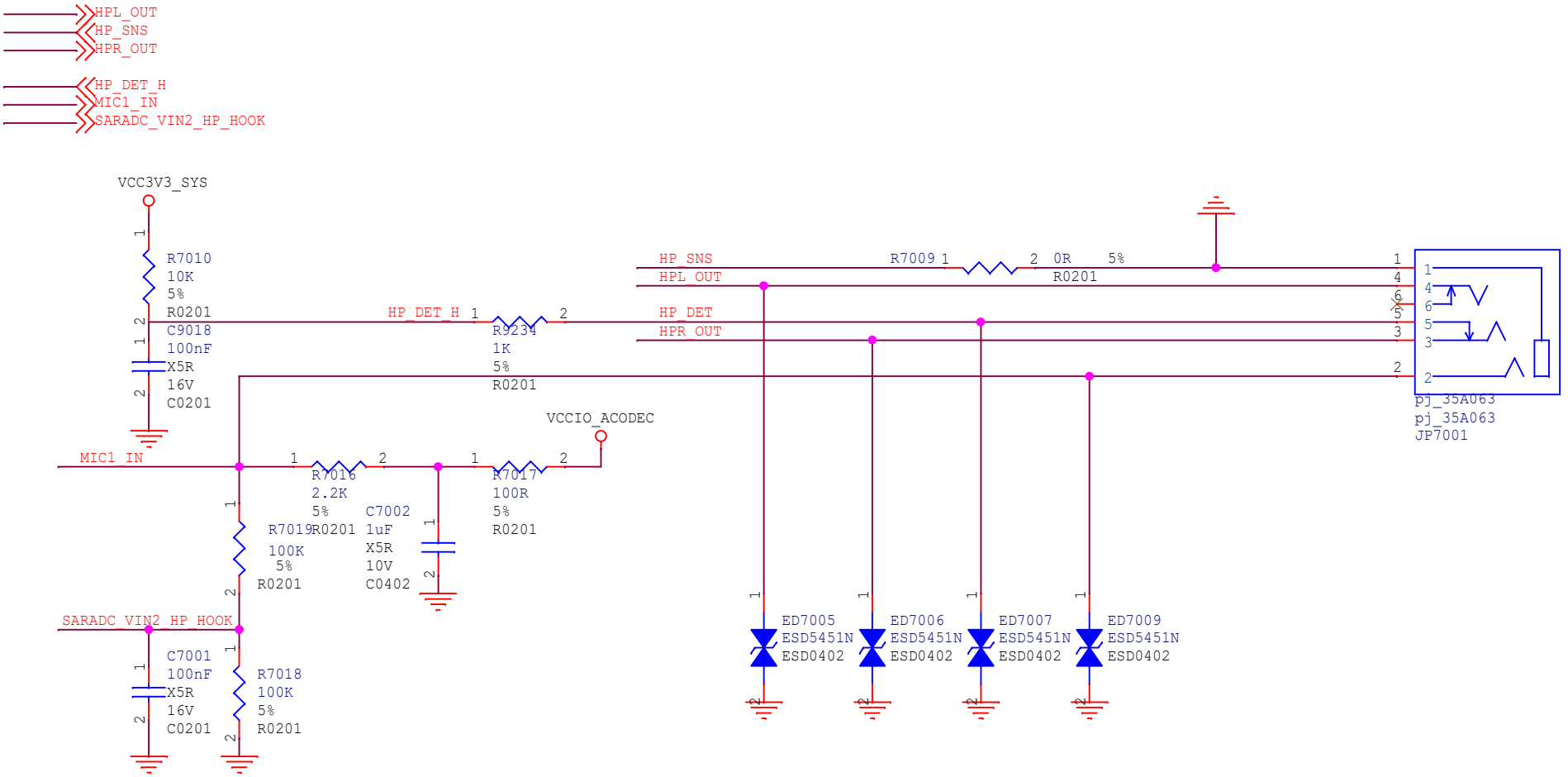
DC-IN 5V



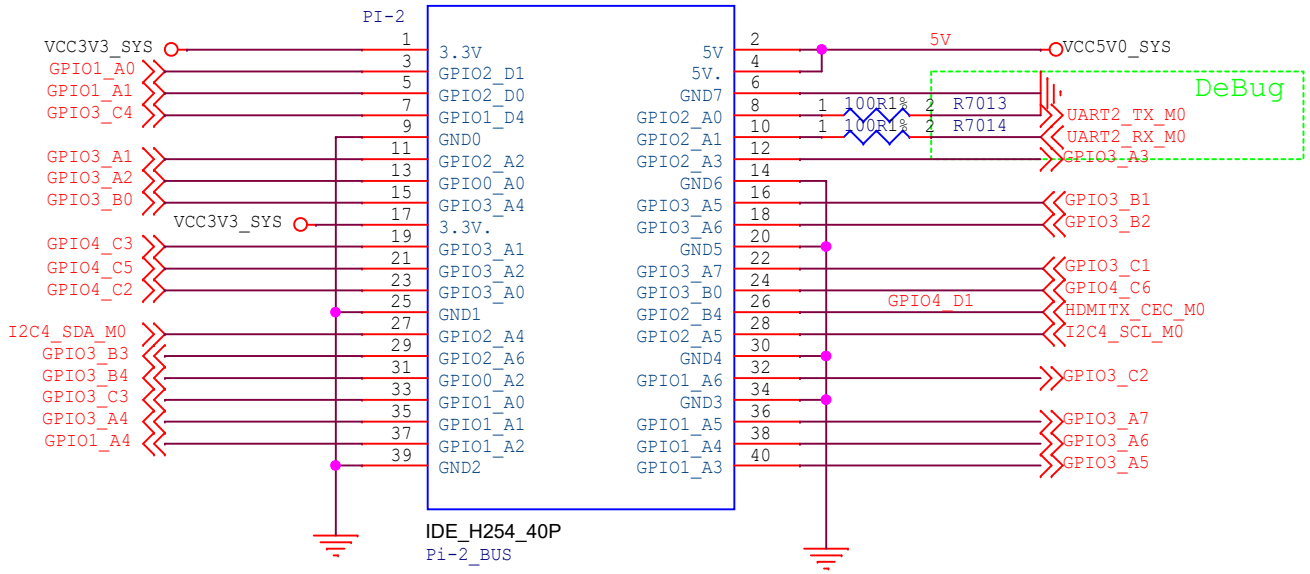
VCC_SYS

PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	20.Power_DC IN				
Date:	Thursday, April 25, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	16 of 30

Headphone Jack

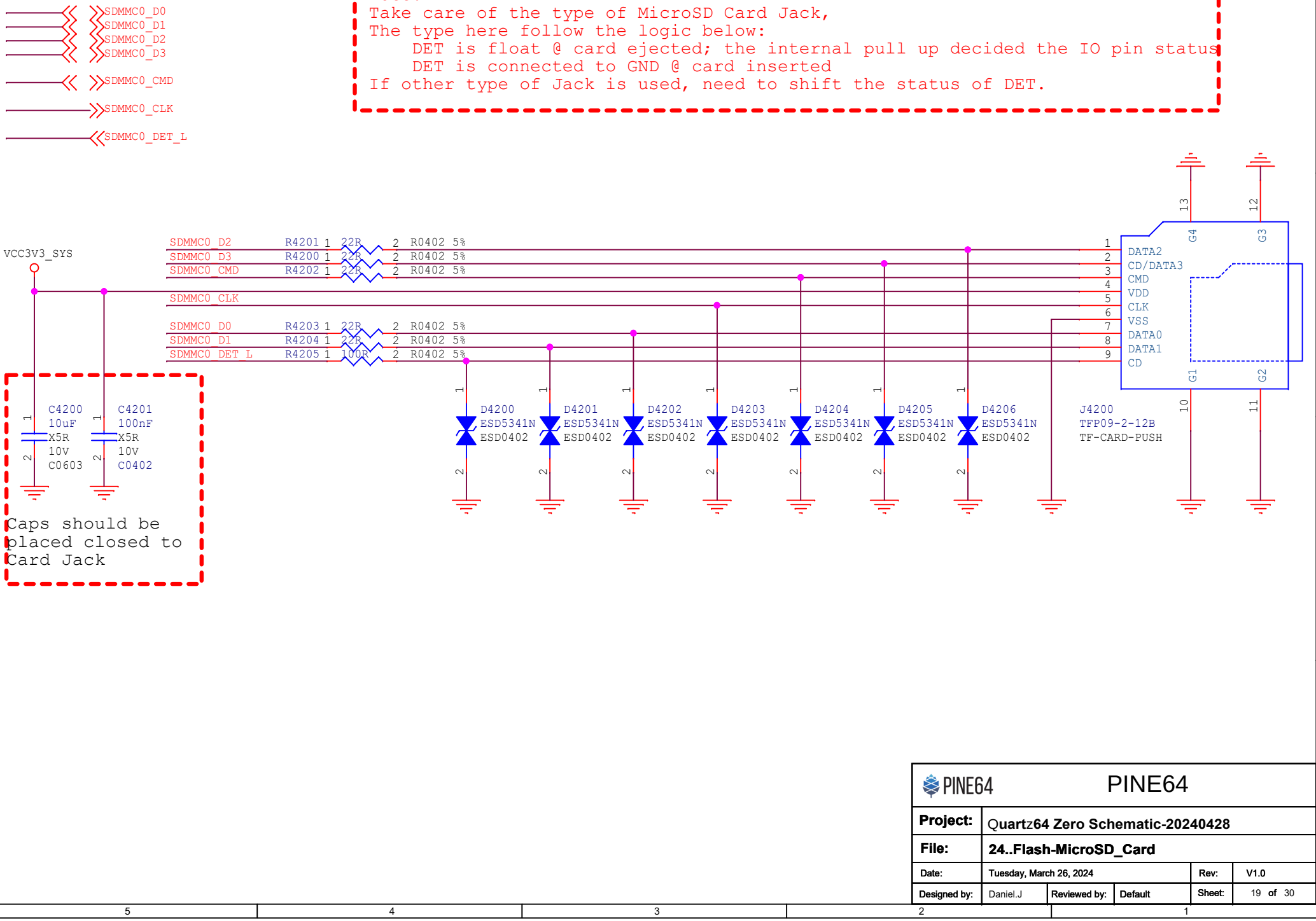


PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	**28.AUDIO**				
Date:	Monday, April 22, 2024			**Rev:**	V1.0
Designed by:	Daniel.J	**Reviewed by:**	Default	**Sheet:**	17 of 30



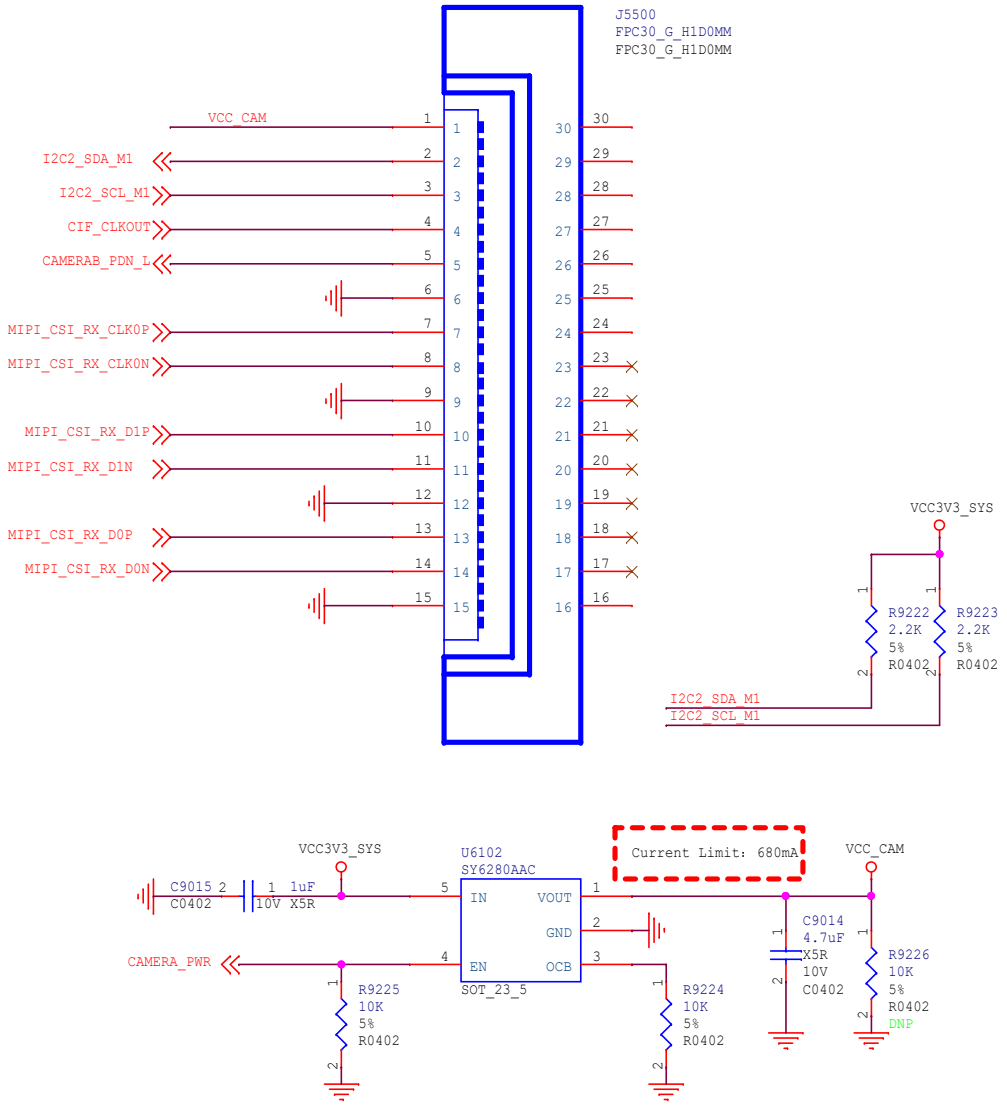
PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	**30.RK3566 PI-2**				
Date:	Thursday, April 25, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	18 of 30

MicroSD Card

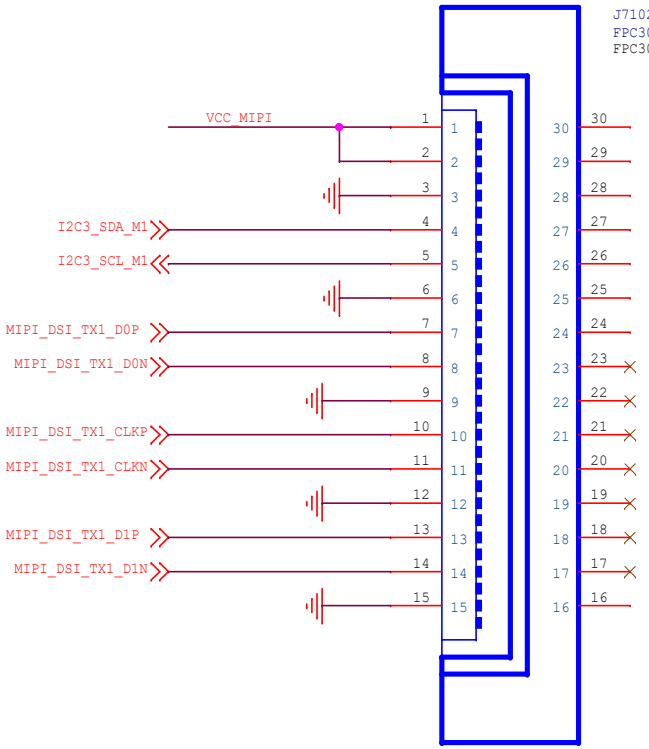


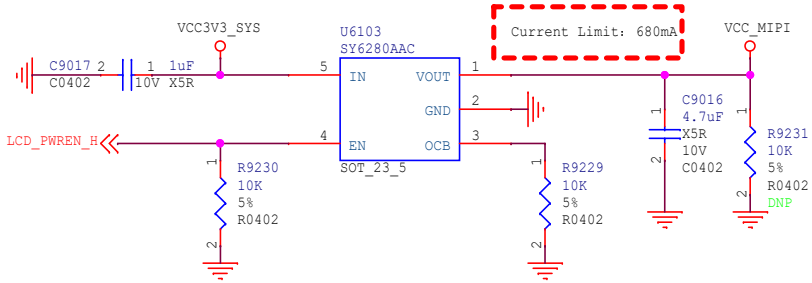
PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	**24..Flash-MicroSD_Card**				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	19 of 30

VI-Camera_MIPI-CSI



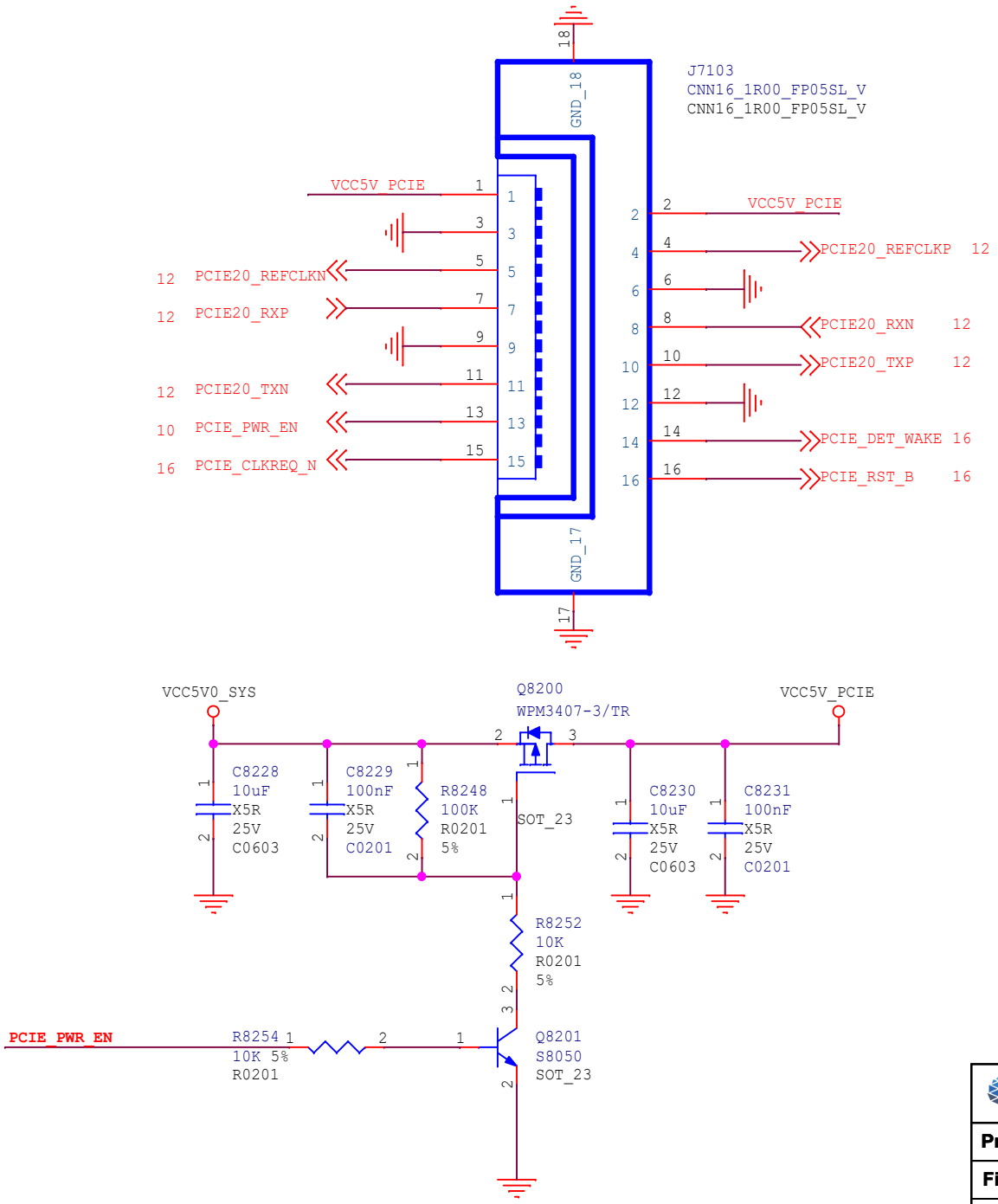
VO-LCM_MIPI-DSI





PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	**31.MIPI DSI/CSI**				
Date:	Friday, April 26, 2024			**Rev:**	V1.0
Designed by:	Daniel.J	**Reviewed by:**	Default	**Sheet:**	20 of 30

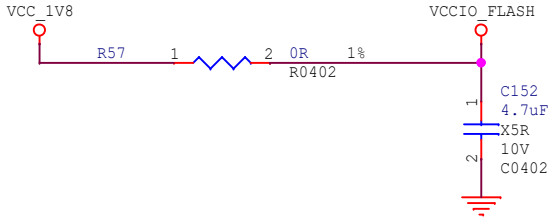
PCIE-M2



PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	**32.PCIe Cnn**				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	21 of 30

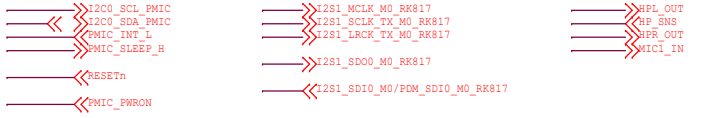
Flash Power Manage

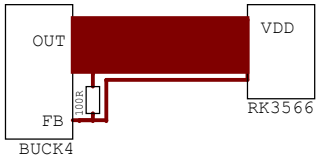
	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)



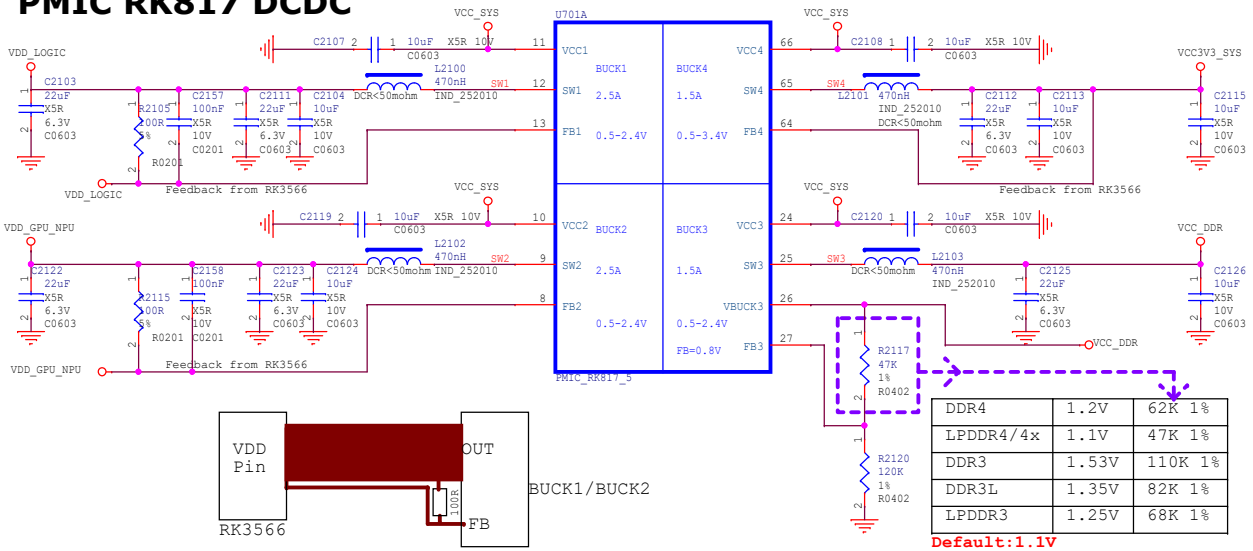
Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	21.Power_Flash Power Manage				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	22 of 30





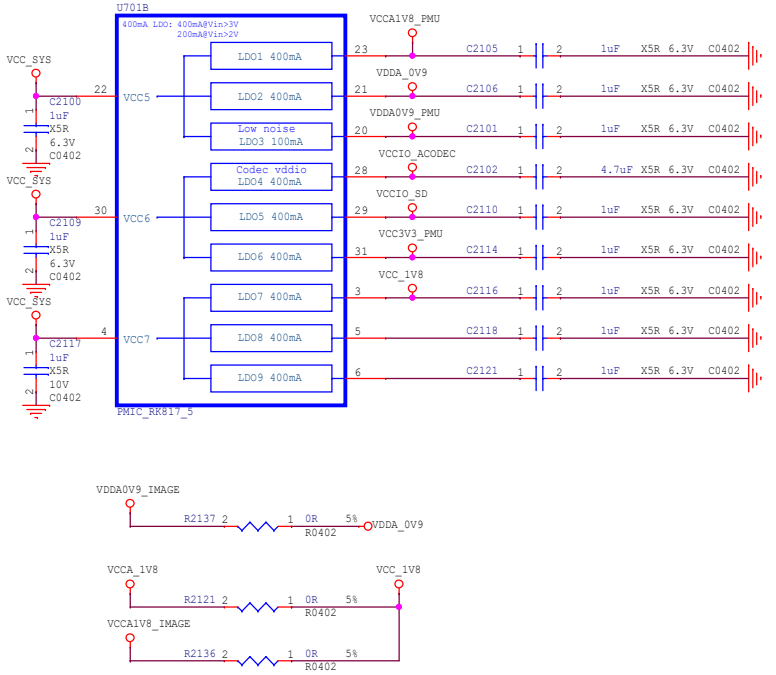
PMIC RK817 DCDC



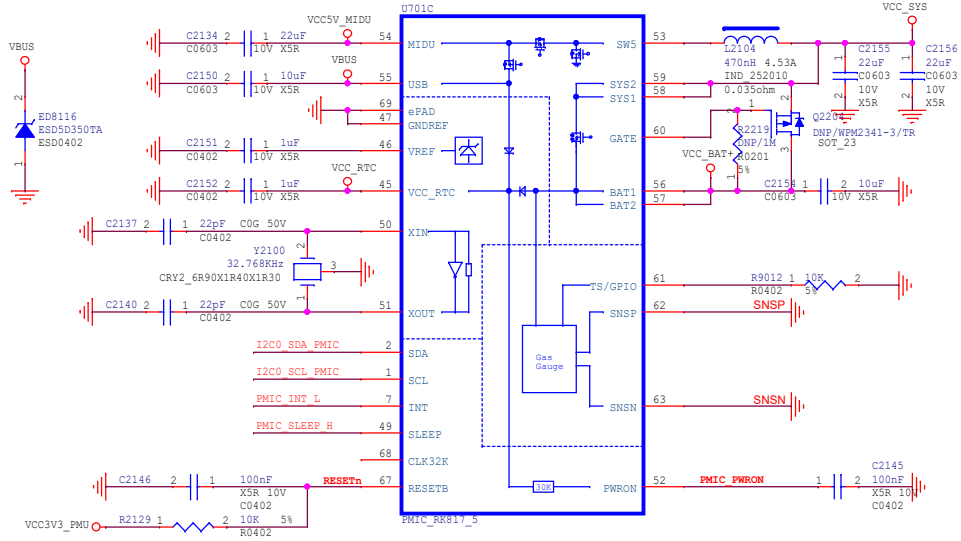
DDR4	1.2V	62K 1%
LPDDR4/4x	1.1V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

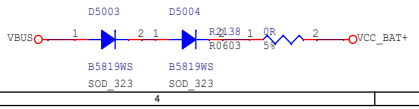
Default:1.1V

PMIC RK817 LDO

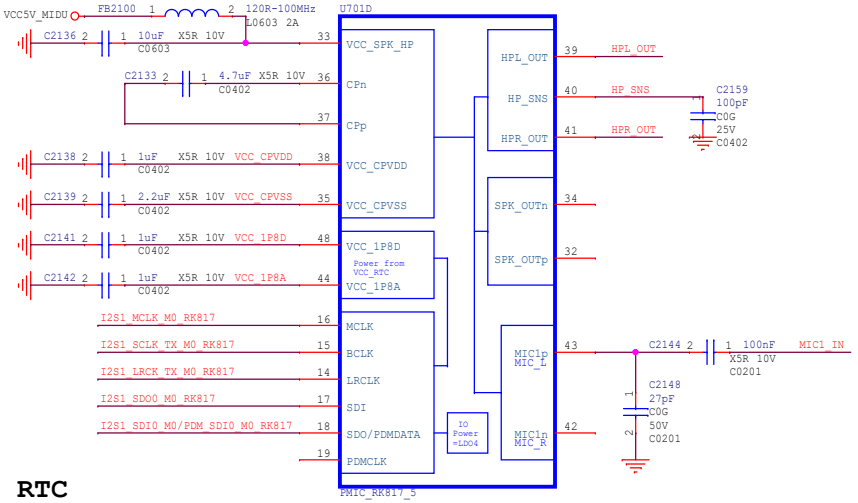


PMIC RK817 Managerment



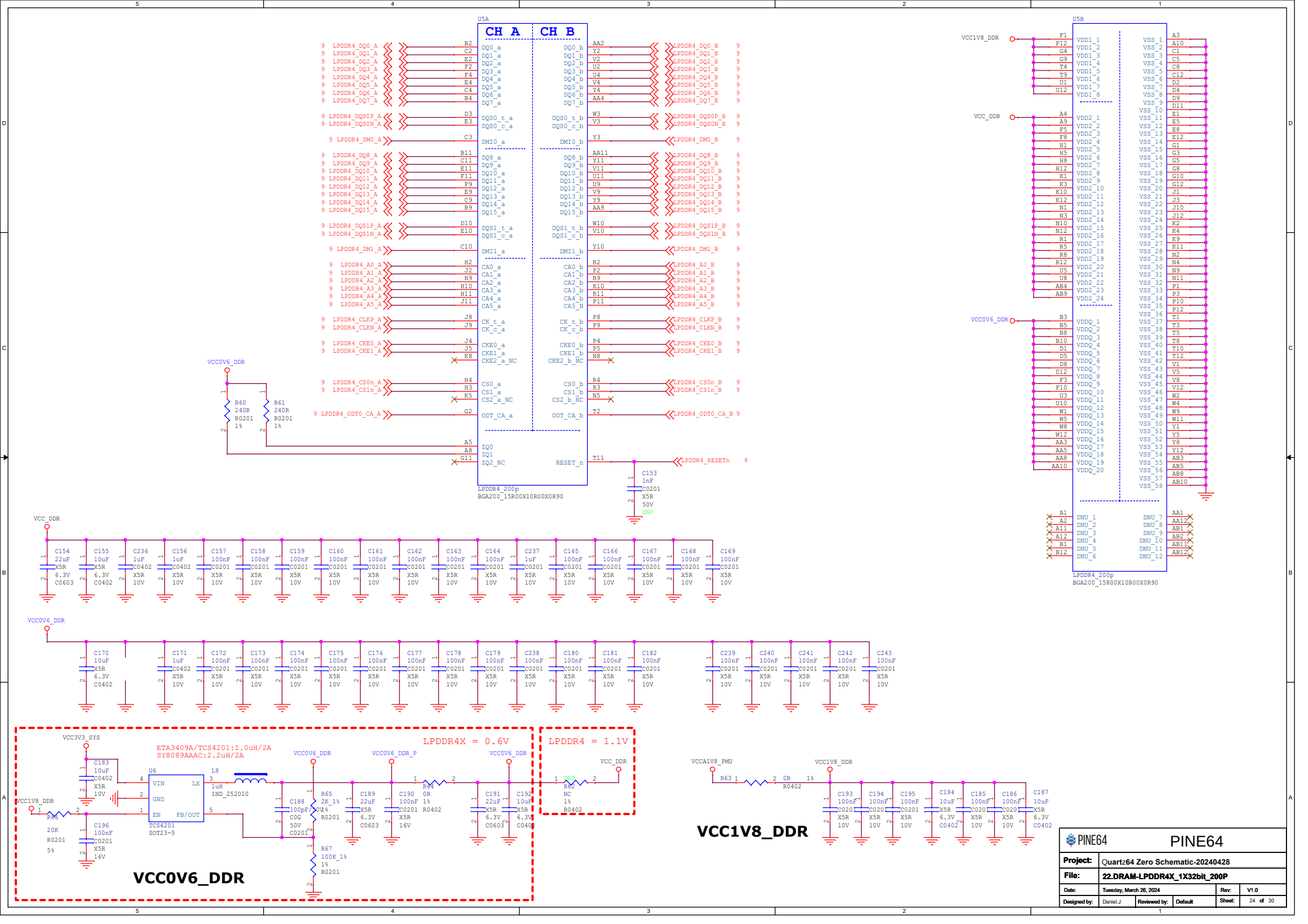


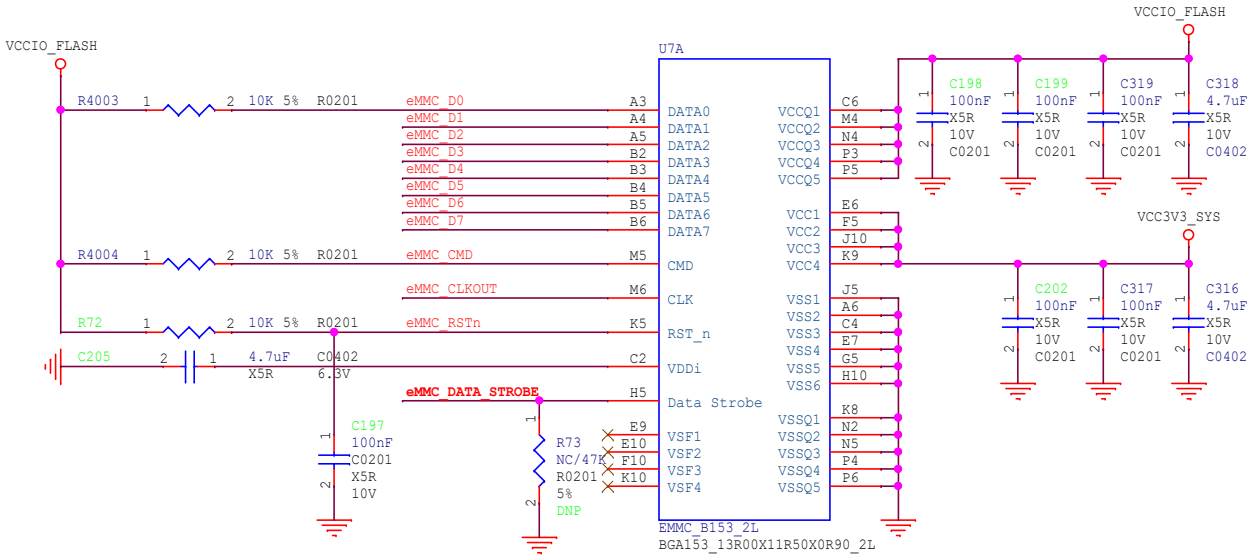
PMIC RK817 CODEC



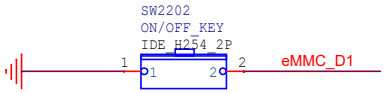
RTC

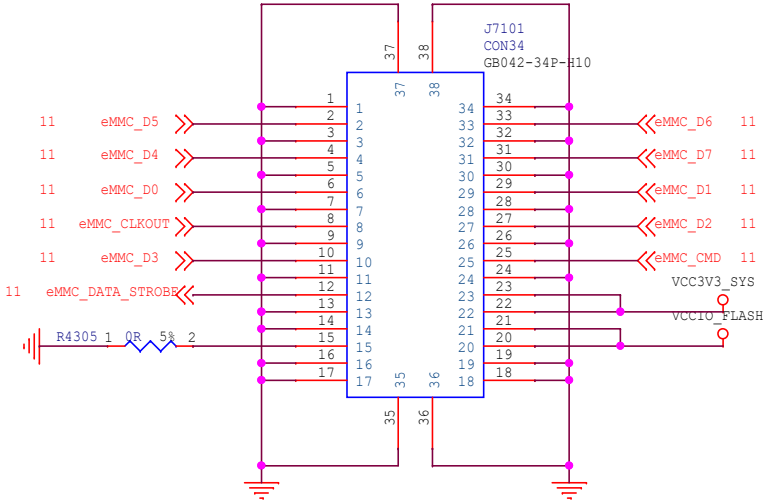
PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	19.Power_PMIC				
Date:	Friday, April 26, 2024			Rev:	V0.1
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	23 of 30

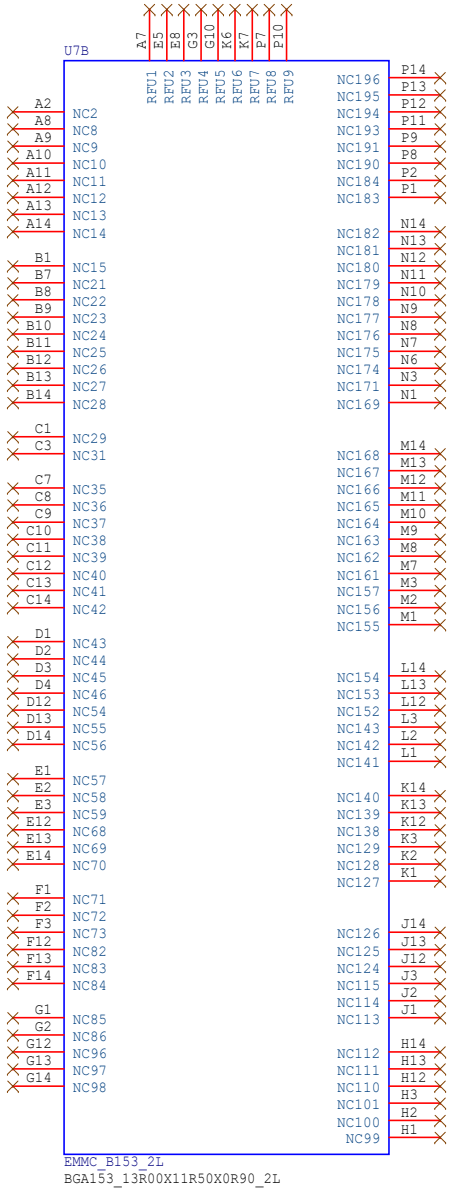

U5A
CH A
CH B
LPDDR4_200p
BGA200_15R00X10R00X0R90
U5B
LPDDR4_200p
BGA200_15R00X10R00X0R90
VCC0V6_DDR
VCC_DDR
VCC1V8_DDR
LPDDR4X = 0.6V
LPDDR4 = 1.1V
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
VCC0V6_DDR
VCC1V8_DDR
PINE64
Project: Quartz64 Zero Schematic-20240428
File: 22.DRAM-LPDDR4X_1X32bit_200P
Date: Tuesday, March 26, 2024
Rev: V1.0
Designed by: Daniel.J
Reviewed by: Default
Sheet: 24 of 30



Note:
disable eMMC







PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	23.Flash-eMMC Flash				
Date:	Tuesday, March 26, 2024			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	25 of 30

HDMI_TX2P_PORT 15,18
HDMI_TX2N_PORT 15,18
HDMI_TX1P_PORT 15,18
HDMI_TX1N_PORT 15,18
HDMI_TX0P_PORT 15,18
HDMI_TX0N_PORT 15,18
HDMI_TXCLKP_PORT 15,18
HDMI_TXCLKN_PORT 15,18
HDMITX_SCL 13
HDMITX_SDA 13
HDMITX_CEC_M0 13
HDMI_TX_HPDIN 15

Cj<=0.4pF

HDMI TX DDC

VCC5V0_SYS
D1
B5819WS
SOD_323
VCC3V3_SYS
R74
10K
5%
R0201
Q1
2SK3018
SOT_323
R75
1.8K
5%
R0201
HDMITX_SCL
HDMI_TXDDC_SCL_PORT
VCC3V3_SYS
R76
10K
5%
R0201
Q2
2SK3018
SOT_323
R77
1.8K
5%
R0201
HDMITX_SDA
HDMI_TXDDC_SDA_PORT

U5000
ESD5304D
SON10_2R50X1R00X0R50
HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
IO1 IO2 GND IO3 IO4
NC_10 NC_9 GND NC_7 NC_6
U5001 ESD5304D SON10_2R50X1R00X0R50

HDMI_TX_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TXDDC_SDA_PORT
HDMI_TX_HPD_PORT
VCC5V_HDMI_TX
ED5000 ESD5341N ESD0402
ED5001 ESD5341N ESD0402
ED5002 ESD5341N ESD0402
ED5003 ESD5341N ESD0402
C5000
1uF
X5R
10V
C0402

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TX_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TX_HPD_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMI_TXDDC_SDA_PORT
VCC5V_HDMI_TX
C356
100nF
C0402
X5R 16V
J2600
XNT-HDMI-001660
HDMI-14_5X11_55-23P

HDMI TX CEC

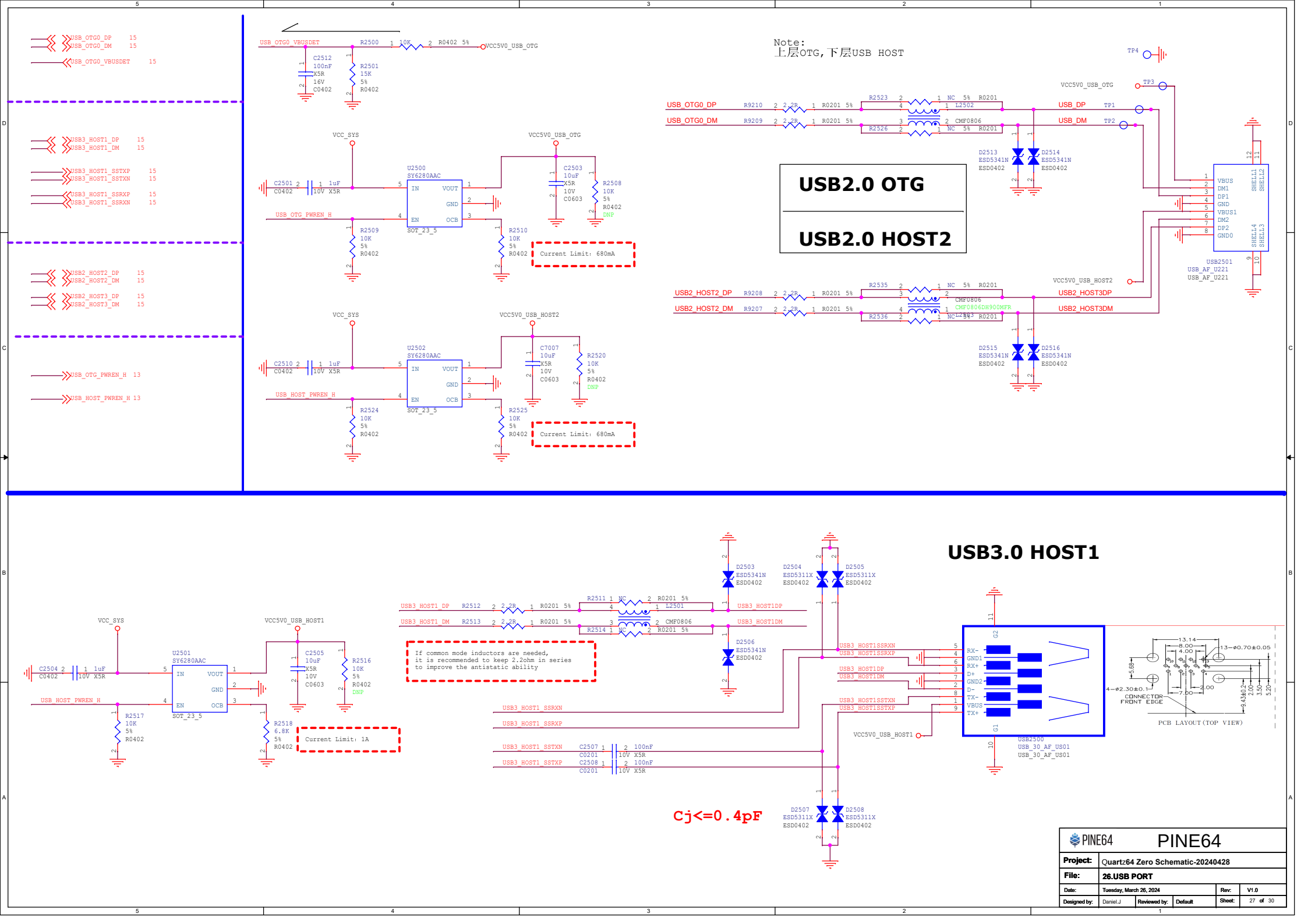
VCC3V3_SYS
VCC5V0_SYS
R79
27K
5%
R0201
Q3
2SK3018
SOT_323
HDMITX_CEC_M0
HDMI_TX_CEC_PORT

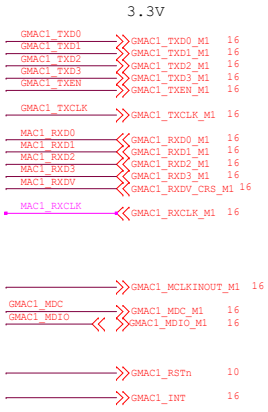
HDMI TX HPD

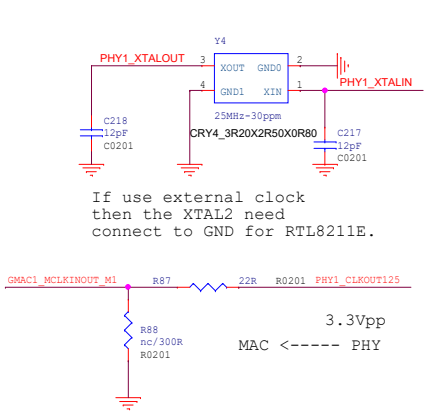
HDMI_TX_HPDIN
R78
1K
5%
R0201
HDMI_TX_HPD_PORT
R80
100K
5%
R0201

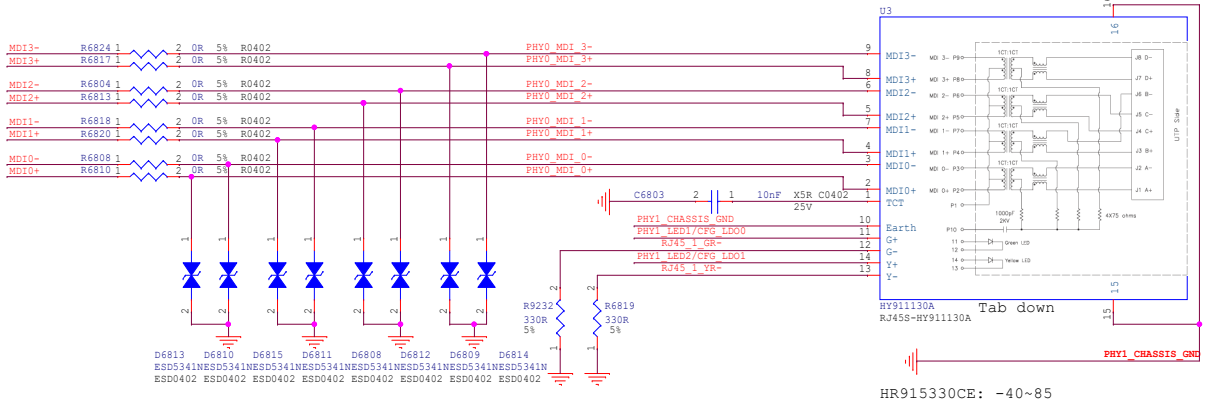
VCC5V0_SYS
D5002
B5819W
SOD_123
VCC5V_HDMI_TX
C5022
1uF
X5R
10V
C0402

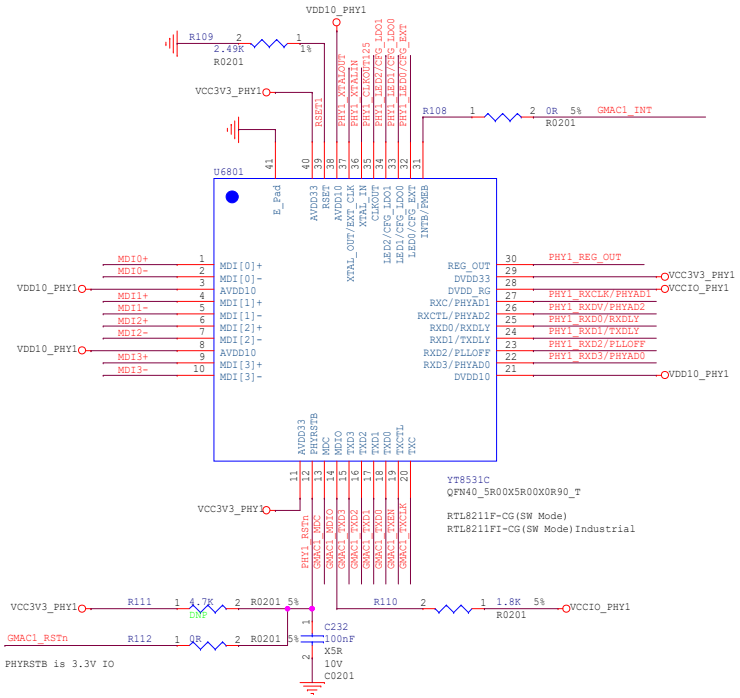
PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	25.VO-HDMI2.0 TX				
Date:	Tuesday, March 26, 2024			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	26 of 30

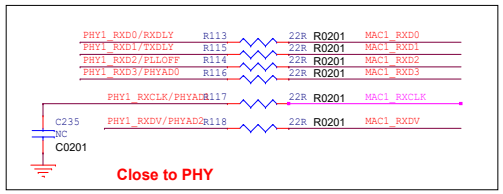

USB_OTG0_DP 15
USB_OTG0_DM 15
USB_OTG0_VBUSDET 15
USB3_HOST1_DP 15
USB3_HOST1_DM 15
USB3_HOST1_SSTXP 15
USB3_HOST1_SSTXN 15
USB3_HOST1_SSRXP 15
USB3_HOST1_SSRXN 15
USB2_HOST2_DP 15
USB2_HOST2_DM 15
USB2_HOST3_DP 15
USB2_HOST3_DM 15
USB_OTG_PWREN_H 13
USB_HOST_PWREN_H 13
USB_OTG0_VBUSDET
R2500 10K R0402 5%
VCC5V0_USB_OTG
C2512 100nF X5R 16V C0402
R2501 15K 5% R0402
VCC_SYS
VCC5V0_USB_OTG
U2500 SY6280AAC
IN VOUT GND EN OCB
SOT_23_5
C2501 1uF 10V X5R C0402
C2503 10uF X5R 10V C0603
R2508 10K 5% R0402 DNP
USB_OTG_PWREN_H
R2509 10K 5% R0402
R2510 10K 5% R0402
Current Limit: 680mA
VCC_SYS
VCC5V0_USB_HOST2
U2502 SY6280AAC
C2510 1uF 10V X5R C0402
C7007 10uF X5R 10V C0603
R2520 10K 5% R0402 DNP
USB_HOST_PWREN_H
R2524 10K 5% R0402
R2525 10K 5% R0402
Current Limit: 680mA
Note:
上层OTG,下层USB HOST
TP4
TP3
VCC5V0_USB_OTG
USB_OTG0_DP R9210 2.2R R0201 5%
USB_OTG0_DM R9209 2.2R R0201 5%
R2523 NC 5% R0201
L2502
CMF0806
R2526 NC 5% R0201
USB_DP TP1
USB_DM TP2
D2513 ESD5341N ESD0402
D2514 ESD5341N ESD0402
USB2.0 OTG
USB2.0 HOST2
VBUS DM1 DP1 GND VBUS1 DM2 DP2 GND0 SHELL1 SHELL2 SHELL3 SHELL4
USB2501
USB_AF_U221
USB2_HOST2_DP R9208 2.2R R0201 5%
USB2_HOST2_DM R9207 2.2R R0201 5%
R2535 NC 5% R0201
CMF0806
CMF0806DH900MFR
R2536 NC 5% R0201
VCC5V0_USB_HOST2
USB2_HOST3DP
USB2_HOST3DM
D2515 ESD5341N ESD0402
D2516 ESD5341N ESD0402
USB3.0 HOST1
VCC_SYS
VCC5V0_USB_HOST1
U2501 SY6280AAC
C2504 1uF 10V X5R C0402
C2505 10uF X5R 10V C0603
R2516 10K 5% R0402 DNP
USB_HOST_PWREN_H
R2517 10K 5% R0402
R2518 6.8K 5% R0402
Current Limit: 1A
USB3_HOST1_DP R2512 2.2R R0201 5%
USB3_HOST1_DM R2513 2.2R R0201 5%
R2511 NC R0201 5%
L2501
CMF0806
R2514 NC R0201 5%
USB3_HOST1DP
USB3_HOST1DM
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
D2503 ESD5341N ESD0402
D2504 ESD5311X ESD0402
D2505 ESD5311X ESD0402
D2506 ESD5341N ESD0402
USB3_HOST1_SSRXN
USB3_HOST1_SSRXP
USB3_HOST1_SSTXN C2507 100nF C0201 10V X5R
USB3_HOST1_SSTXP C2508 100nF C0201 10V X5R
Cj<=0.4pF
D2507 ESD5311X ESD0402
D2508 ESD5311X ESD0402
RX- GND1 RX+ D+ GND2 D- TX- VBUS TX+
USB2500
USB_30_AF_US01
CONNECTOR FRONT EDGE
PCB LAYOUT(TOP VIEW)
PINE64
Project: Quartz64 Zero Schematic-20240428
File: 26.USB PORT
Date: Tuesday, March 26, 2024
Rev: V1.0
Designed by: Daniel.J
Reviewed by: Default
Sheet: 27 of 30

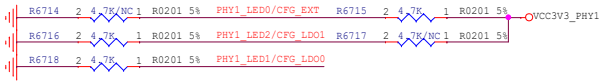




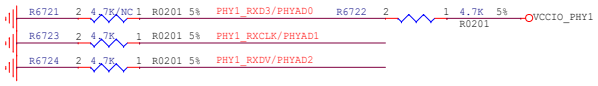


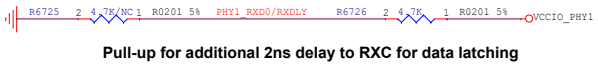


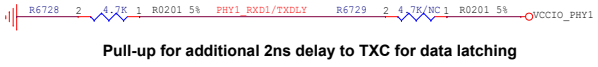


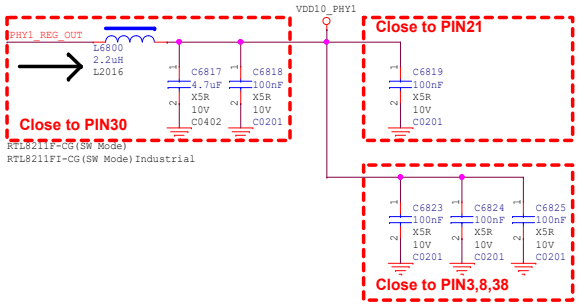


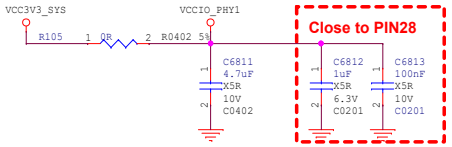
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V (default)	1'b0	2'b10	

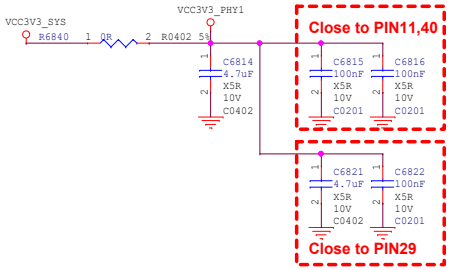












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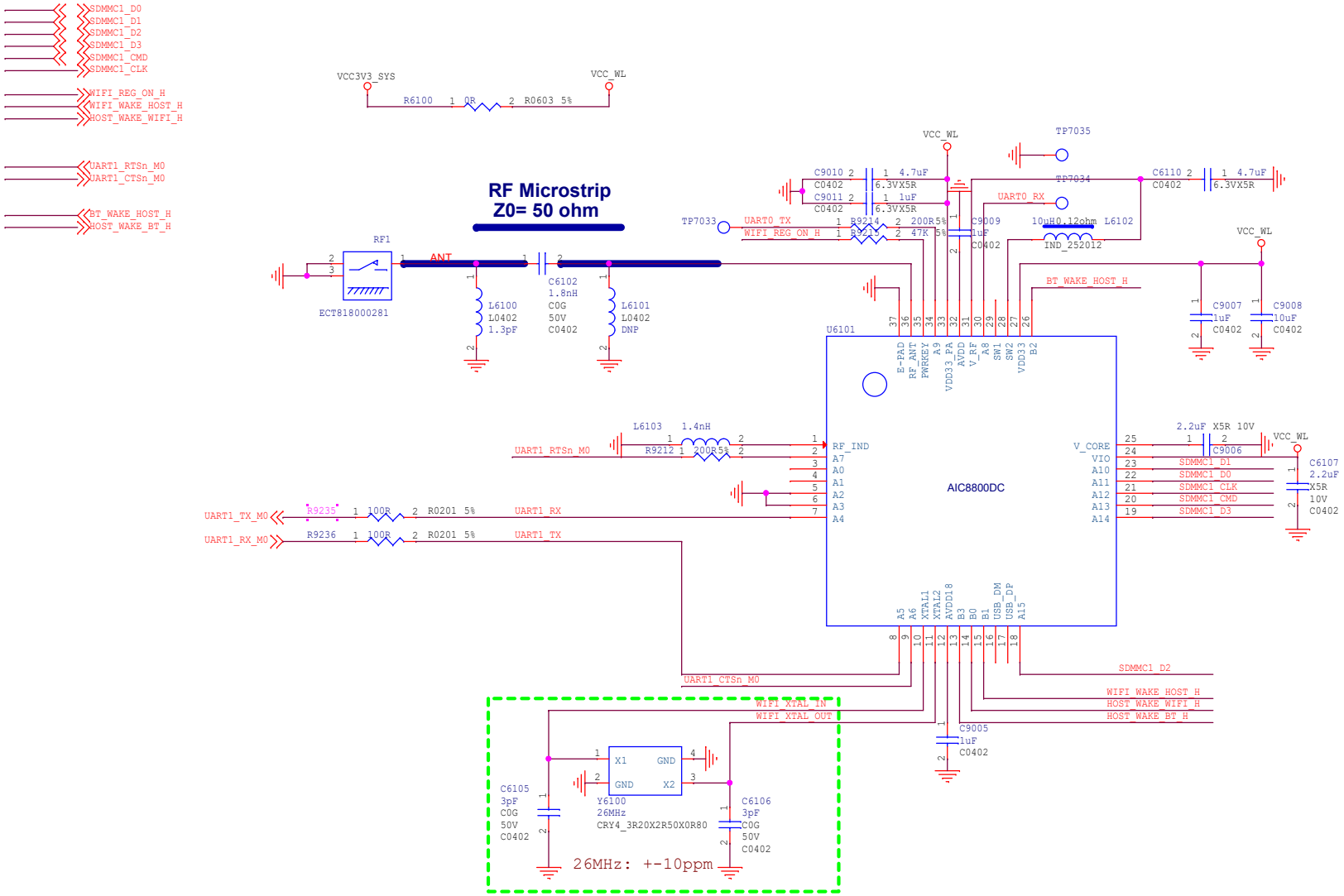
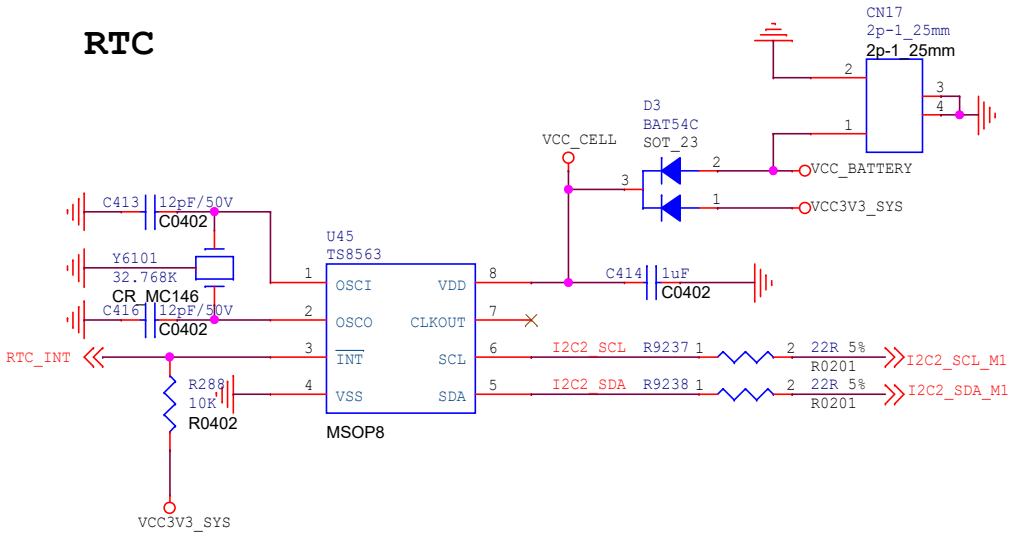
Title:	1000M-PHY		
File:	Quartz64 Zero Schematic-20240428	REV:1.0	
Create Date:	Tuesday, April 13, 2021	Page Num:	28
Modify Date:	Tuesday, March 26, 2024	Page Total:	30

SDIO WIFI/BT Module-1T1R

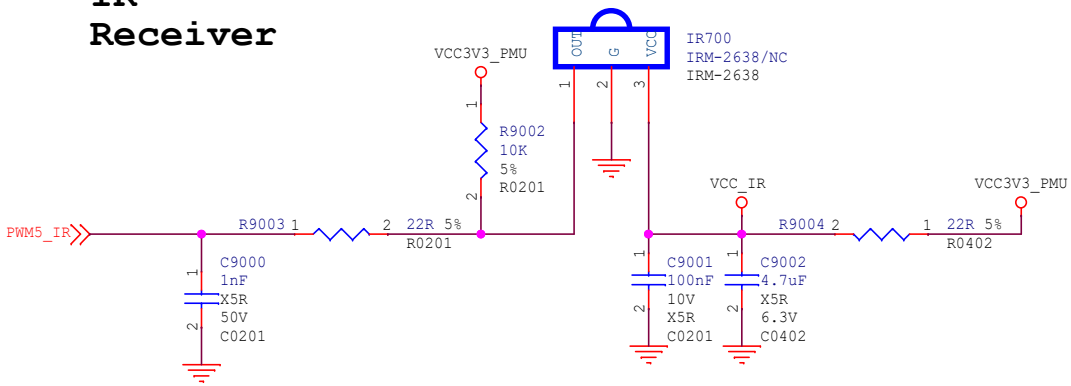


PINE64	PINE64				
Project:	Quartz64 Zero Schematic-20240428				
File:	29.WIFI				
Date:	Wednesday, April 24, 2024			**Rev:**	V1.0
Designed by:	Daniel.J	**Reviewed by:**	**Default**	**Sheet:**	29 of 30

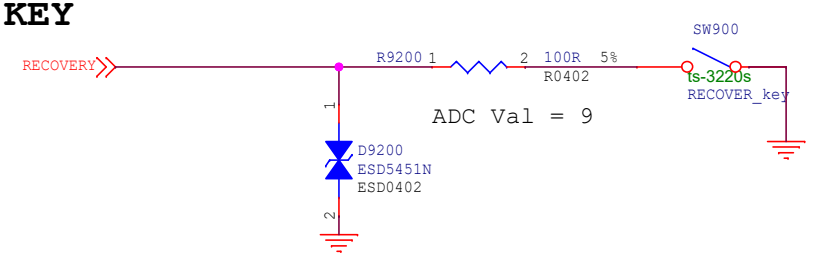
RTC

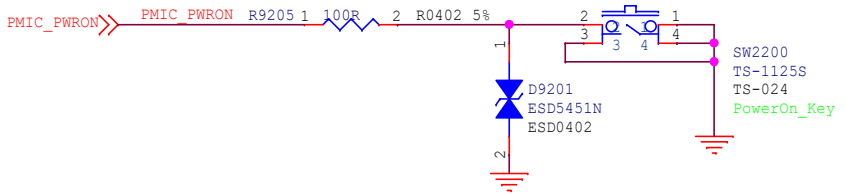


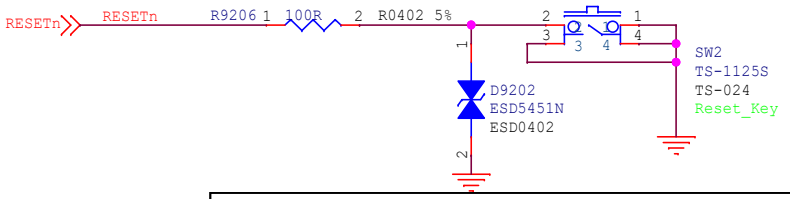
IR Receiver



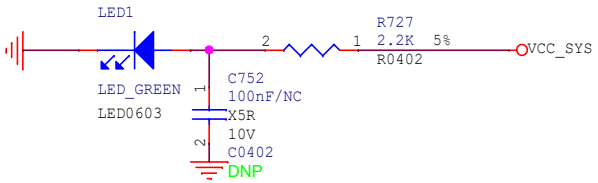
KEY

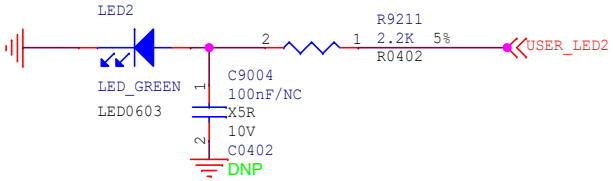






电源指示灯（绿色）





Working LED(白色)

PINE64	PINE64	
Title	Quartz64 Zero Schematic-20240428	
Size	Document Number: LED, Key, and IR	Rev: 1.0
Date: Sunday, April 28, 2024	Sheet 30 of 30	